Vixar Application Note

VCSEL Pulse Driver Designs for ToF Applications

1 Introduction

There are many ways to enable control the activation of a VCSEL diode. Being current-controlled devices, many methods of constant current sourcing and high-speed current switching are available. Like LEDs, VCSELs can be powered in continuous wave (CW) mode with a constant current sink. A FET can be incorporated in series to allow for PWM control of the VCSEL for long pulse width (> 100 us) applications.

One of the main advantages of VCSELs is the significantly reduced rise times possible (< 1 ns) that allow for extremely short pulse widths essential for Time of Flight (ToF) in LiDAR applications. In order to realize these benefits, the circuit must enable high current switching by reducing in-series resistance and parasitic inductances both inside the components and the overall circuit design.

This application note focuses on addressing the specifics behind high-speed driving conditions (n-pulse range) that maximize the VCSEL's potential in ToF designs. The theory behind design constraints and major sources of error are covered. Additional material is presented for both low and high-power scenarios where additional design decisions are necessary for both applications.

2 Design Theory

High speed VCSEL design can be summarized with a few essential components required for operation [Figure 1]. The VCSEL is powered by a bank of capacitors that enable instant charge delivery. A low-resistance FET enables switching of high forward currents. The FET is typically controlled with a Gate Driver that's triggered by a low input signal.

2.1 Schematic Components

The VCSEL itself can be roughly modeled as an ideal diode with a specified level of resistance, capacitance, and inductance. As a rule of thumb, larger die will have higher capacitance values and lower inductance values due to larger bond pads and higher quantity of wire bonds for electrical connectivity.

The FET is typically modeled as having a series resistance between the drain and source that is dependent on the charge present at the Gate. The gate can be modeled as a capacitor between the source and drain. While the gate does not require significant power to activate the FET, enabling fast carrier delivery to the gate on the scale of Amps in a sub-nanosecond time frame is essential for high-speed VCSEL activation.

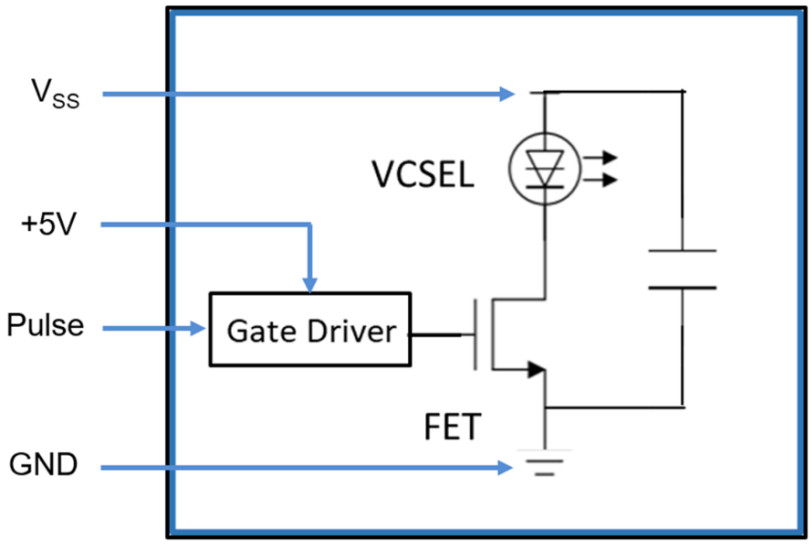

Figure 1: A circuit for high speed operation of a VCSEL laser for short (ns) pulse width operation.

The gate driver is typically designed as a dual-sided high/low MOSFET pair that controls fast charge sourcing/sinking to the FET gate. To improve signal speed, the MOSFETs are controlled through a comparator activated by a differential input signal. It is also necessary to add capacitors in close proximity to the gate driver's power pin to ensure swift carrier availability for current delivery to the gate.

For high-pulsed operation, the majority of the current during VCSEL pulses is delivered from the capacitor bank in close proximity to the VCSEL anode. If the design requires 100 A of current in a 10 ns pulse, the capacitor bank must have at least 1 µC of charge stored before FET activation. Many applications require pulse trains of multiple ns pulses in quick repetition, where there is not enough time between individual pulses to fully charge the capacitor bank. Thus, the total capacitance must store enough charge to supply the entire pulse train between recharge frames.

2.2 Design Inductance

Inductance is the main cause of slow rise times in VCSEL pulse widths. As described by circuit theory, the rate of current rise over time is dependent on two factors: voltage and inductance. The relationship can be seen in equation (1). Inductance is inherent in all system designs, and even sub nH designs have an impact on high peak powers. A simple way to increase rise times in laser pulses is to increase the driver voltage across the VCSEL and FET. However, design rules must

be met to pick out the appropriate components and required PCB layouts to handle increased voltage thresholds. This may be counter-intuitive, as these precautions will ultimately increase the inductance of the system.

$$V = L\,\frac{di}{dt} \tag{1}$$

In general, it is best to reduce system inductance through board design and component selection. It is ideal to minimize the current loop length between the capacitor bank, VCSEL, and FETs. Capacitors themselves can be a source of inductance and utilizing a bank of multiple low ESL (equivalent series inductance) ceramic capacitors can improve rise time.

A significant source of inductance comes from wire bonds used to connect the anode on top of the VCSEL die [Figure 2]. A single wire bond exhibits roughly 1 nH of inductance. The overall inductance can be reduced by adding more wire bonds. This effectively adds inductance in parallel and reduces the overall inductance. It is advantageous to use as many wire bonds as possible to improve current flow and reduce parasitic inductance.

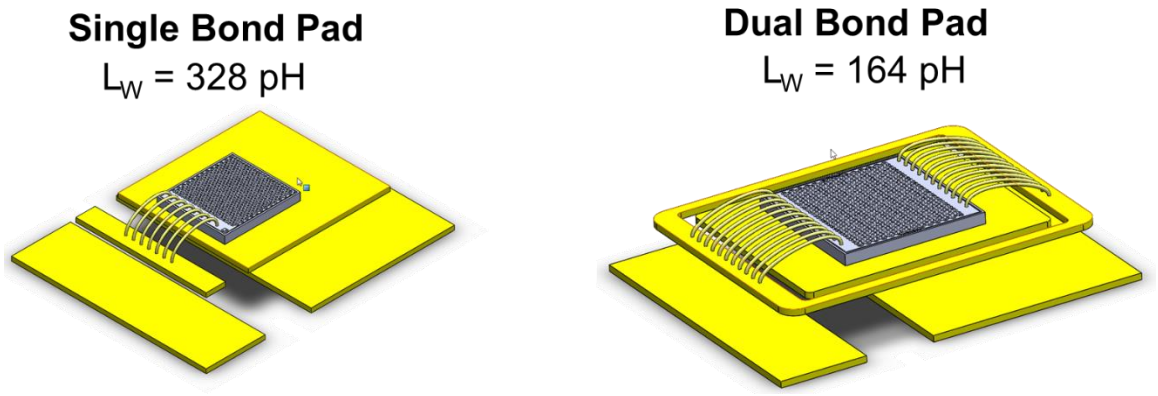

Figure 2: Simulation results of wire bond inductance of single bond pad VCSEL with 7 wire bonds (left) and dual bond pad VCSEL with 20 wire bonds (right).

This is one of the attractive features of flip-chip VCSELs, where both cathode and anode are bonded directly onto the substrate without requiring wire bonds. If the VCSEL is bonded directly on the VCSEL driver, then the current loop between laser, driver, and capacitors is minimized and all packaging inductance is nonexistent.

2.3 Rise and Fall Time

For most cases, end users want to know the time it takes for the optical pulse to transition from OFF to ON. Due to the many different shapes a pulse can have, rise time is typically determined as a measurement as percent of peak power. Some common measurement criteria are the time it takes to get from 10% to 90% max power, while others will utilize 20% to 80% max power to remove more transient noise from the measurement region.

Due to the nature of inductance, rise time will be dependent on maximum current to achieve the desired power. The circuit design typically controls how fast the current can be increased and is measured as the rate of current increase (di/dt) and is determined by the inductance in the circuit. This rate will define the time it takes to reach the max current levels. In most cases, rise time is not a factor of the VCSEL die, but rather the circuit design and packaging along with the laser driving conditions.

Rise and fall times will differ based on the circuit design. When the VCSEL cathode is pulled high or low by the laser diode driver, the current path may take different paths in the circuit. Typically, enabling current flow through the VCSEL exhibits more inductance due to the larger current path from the capacitors. Circuit designs can reduce the current loop when the VCSEL is turned off and improve signal fall time. In general, VCSEL rise times are typically larger than fall times.

2.4 Timing Delay

In addition to a finite rise time associated with the signal, there is also a time delay present between the input signal and the activation of forward current through the VCSEL. Most of the delay is present from activation delay through the gate driver and charge delivery to the FET's gate. High-speed gate drivers still exhibit >1ns timing delays between when the system receives the analog signal and when the VCSEL experiences a forward current and irradiates optical power.

The best method of determining VCSEL activation is by monitoring the voltage at the FET drain. A drop in voltage verifies when the gate is finally activated and current starts flowing. This signal becomes the clock for a Timing Alignment (TAL) signal to sync the illumination source with a TOF detector.

3 Low Power Driver Design

Many applications need a small optical signal (< 5 W) to illuminate any objects near the laser source. For VCSELs having a slope efficiency (SE) of at least 1 W/A, this requires a driver that delivers peak pulse currents up to 5 A. For these low power designs, silicon-based driver

solutions are a cost-efficient method in controlling pulse shape and maintaining constant current. Drivers in the form of ASICS can add additional capabilities that can be integrated and programmed into the laser diode driver.

ASICs can be designed with several attractive features [Figure 3]. Inputs for thermistor monitoring can allow for power adjustments or enable emergency shutdowns to prevent permanent thermal damage. Monitoring diffuser health with a photodiode or conductive interlock can ensure that the laser beam is being diffused and eye safe. Modules can be coded with calibration data that is measured and downloaded during production. ASICs can also enable adaptive power controls to adjust to the environment or different software protocols

Another advantage with ASICs is the flexibility in packaging. This enables the VCSEL to be integrated in close proximity to the driver to minimize inductance. The VCSEL die could be mounted directly on the laser driver package. The integration of flip-chip VCSELs directly on ASIC drivers can eliminate the need for wire bonds and eliminating most parasitic inductance in the circuit design. The main concern with this solution is that thermal dissipation of the VCSEL must travel through the ASIC, which is also a source of heat in the system.

Many ASIC drivers have multiple current channels, each equipped with a FET and gate driver, that can be individually controlled for addressability. All channels can be combined to further increase the pulse current of a single laser source. Thus, increasing effective current typically involves multiple Si FETs in parallel. Regardless, silicon-based ASICs are typically limited to a < 10 Amps of pulsed current for ToF applications.

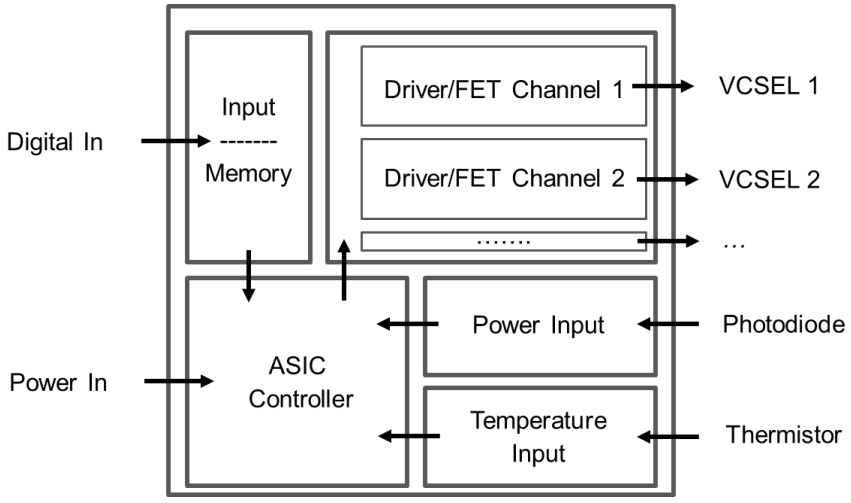

Figure 3: An ASIC driver for VCSELs can contain many capabilities, including multiple driver channels, power monitoring, and temperature correction.

4 High Power Driver Design

Many VCSEL-based ToF applications are expanding their monitoring capabilities and require significantly higher levels of optical power spread out farther distances over a wider field of view. When a laser diode needs more than 5 Amps of driving current, Si-based ASICs become more difficult in design to handle the higher current loads. The large size required to develop a low resistant FET becomes a limit in overall pulse performance. Thus, alternative solutions become attractive for high power drivers as the material properties determine the minimum FET size.

Recently, FETs developed with Gallium Nitride (GaN) technology have shown to exhibit resistance levels magnitudes lower than Si and can handle significantly higher currents in a condensed footprint package. This also reduces the parasitic capacitance and improves switching speed and efficiency. GaN-based FETs are typically stand-alone parts and must be connected to an appropriate FET driver to deliver enough current to the gate and ensure fast switching speeds. Multiple components need to be populated for an effective VCSEL driver module, and insight is necessary for an efficient design.

4.1 GaN FETs

Most GaN FETs can be treated very similarly to a Silicon power MOSFET. Current flows from the drain to the source if a voltage is applied to the gate. The gate acts as a capacitor between the drain and source, and the drain current will rise at the rate at which the gate accumulates charge.

The source-drain current is dependent on both the supply voltage at the drain and the gate charge. To improve rise times, the supply voltage that delivers current through the VCSEL and FET is adjusted to counteract parasitic inductance and to improve rise times. Supply voltages can range from 10 V for industrial 3D cameras to >50 V for long-distance LiDAR applications. In contrast, the gate voltage for most GaN FETs have a maximum rating of ~5 V. Thus, two separate power lines must be designed for fast and powerful laser operation.

Due to inductance effects for high current applications, current spiking may be present due to fast switching speeds. These transients can be lethal to the electronics, including the GaN FET. Thus, it is advised to add a RC snuffer circuit across the FET drain and source. If the RC constant is too large, it will interfere with the switching speed of the laser system. The RC circuit must be optimized to protect the FET while minimizing impact of laser pulse performance.

4.2 Gate Drivers

Switching the FET requires a significant amount of charge at the gate in a narrow time window for narrow pulse widths. Gate drivers act as a signal amplifier to both improve charge delivery to the FET's gate during activation and the depletion of charge from the gate when deactivated. Gate drivers are highly optimized to ensure fast propagation delays and minimum pulse widths.

For optimal operation, the gate driver does require a low ESR capacitor near the device for instant charge delivery to the GaN FET.

Gate drivers typically consists of two components: a trigger and a FET structure [Figure 4]. The trigger may take a single PWM signal or a differential signal to activate charge delivery to the GaN FET. The trigger output drives a pair of internal FETs to control the charge at the FET's gate. At least two FETs are required to ensure fast delivery and depletion of gate charge for short rise and fall times respectively.

The gate of the GaN FET is also susceptible to potential transients in the charge delivery pulse. Since the gate acts as a capacitor to hold charge, low value resistors can be inserted before the FET gate to create an RC circuit to minimize electrical overstress on the FET during high switching frequencies, but high value resistors will directly impact rise and fall times of the VCSEL pulse. For lower power applications, these gate resistors may not be necessary based on the FET's internal characteristics.

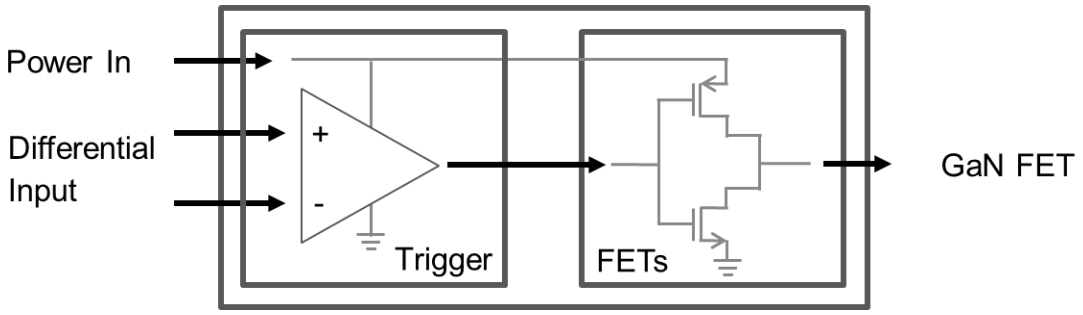

Figure 4: A gate driver illustration that consists of a trigger and a pair of FETs.

5 VCSEL Performance

VCSEL performance is limited to thermal buildup inside the die. The VCSEL's maximum optical output power is reached when the die's junction temperature is ~ 150 C. This is the point of thermal rollover, where additional current will decrease the output power of the VCSEL. For short ns pulse widths, the total dissipated power per pulse is insignificant enough to raise the VCSEL junction temperature. This allows for significantly higher pulse currents. Sufficient time should be allowed for VCSEL cooldown between pulses to prevent cumulative thermal buildup.

Slow rise and fall times not only degrade ToF performance, but they add additional thermal buildup in the die due to the additional time required to meet peak power requirements. While rise times can be increased by increasing the supply voltage, as shown in equation (1), this is typically not desirable for many practical reasons, including PCB layout, component selection, and power supply requirements. Thus, minimizing rise time is best achieved by minimizing parasitic inductance through electrical design and by reducing forward currents with multi-junction VCSEL technology [Figure 5].

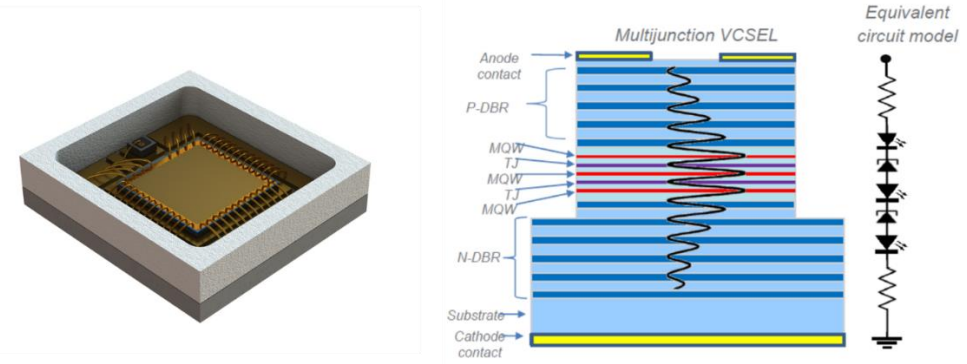

Figure 5: Methods used to improve rise times is to maximize the amount of wire bonds to reduce inductance (left) and utilize multi-junction VCSELs to reduce the driving current (right).

The main source of VCSEL parasitics comes from the wire bonds. While larger die can deliver higher power levels, they can also be designed with multiple bond pads to allow for more wire bonds. Vixar currently produces a 2mm x 2mm VCSEL die (1672 apertures) with 4 wire bond pads surrounding all edges of the VCSEL to allow for > 50 wire bonds.

Multi-Junction VCSELs are another technology that can overcome additional many of the limitations in narrow pulse widths. By increasing the number of active regions, the overall gain inside the cavity can be improved. While this increases the voltage requirements of the driver, significantly less current is needed to achieve optical power targets. Thus, rise and fall times can be significantly reduced by a factor of how many active regions the VCSEL contains.

Multi-junction VCSELs have demonstrated superior power density performance compared to their single junction counterparts. They achieve higher peak powers and improved wall plug efficiency for short pulse widths. These improvements come with the cost of a higher driving voltage and a wider beam divergence. Thus, many factors need to be considered when deciding an appropriate VCSEL technology for TOF applications.

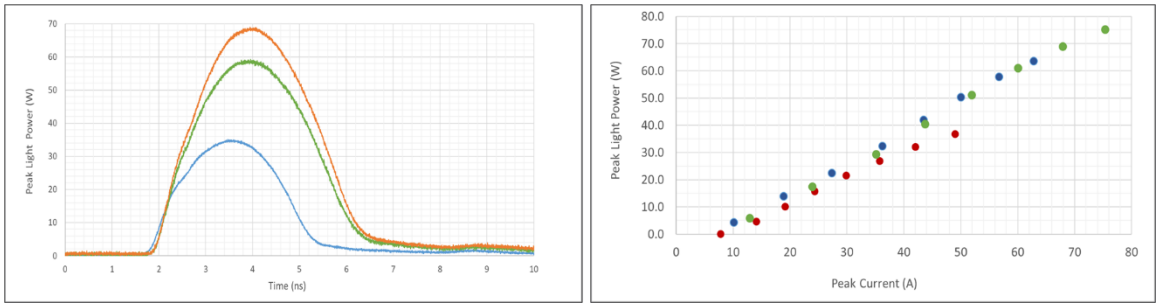

Figure 6: Measurement results of a 2mmx2mm VCSEL (1672 apertures) pulsed at 4 ns with a resonant laser driver, demonstrating fast rise times (left) and high peak powers (right).

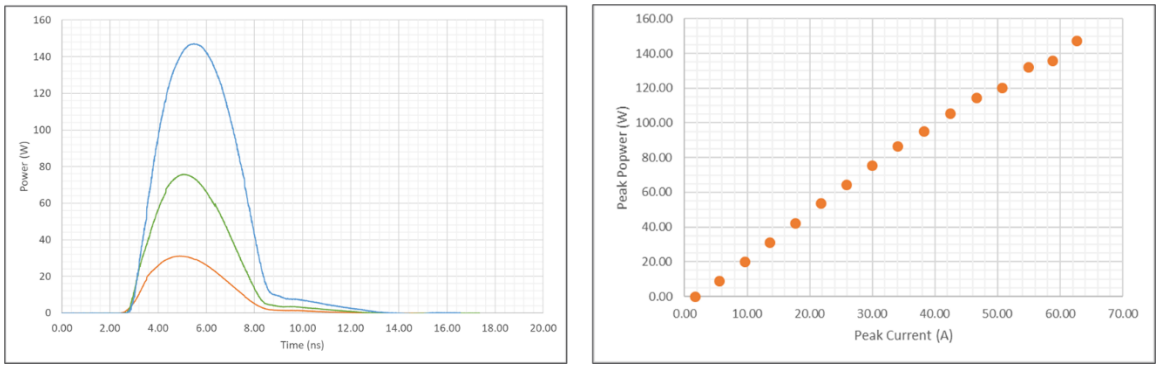

Figure 7: Measurement results of a multi-junction (3J) VCSEL (281 apertures) pulsed at 5 ns with a resonant laser driver, showing fast rise times (left) and high peak powers (right).

6 Conclusions

For ToF illumination, driver design criteria must be taken into consideration for ns pulse widths. VCSELs require low parasitic inductance for short rise times and high peak powers. This includes the selection of proper storage capacitors, high-speed FET switches, and compact circuit design. Low power VCSELs can be driven with ASICs with many integrated features, including diffuser monitoring, thermal management, and module calibration. Higher power applications require more discrete components including a GaN FET and a gate driver to deliver high current loads to the VCSEL.

Vixar has developed and proven VCSEL solutions for ToF applications, including higher power VCSEL die layouts and multi-junction VCSEL technology. Vixar has shown that multi-junction VCSELs can produce >100W of optical power with short rise times for ToF applications.