Vixar Application Note

VCSEL Die Handling and Packaging

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1 Introduction

Vertical Cavity Surface Emitting Lasers (VCSELs) are top-emitting sources and can be wafer-probed before dicing, sorting, and packaging. This allows for VCSELs to be easily packaged into many different form factors. While most EEL-based semiconductor lasers have traditionally been mounted in transistor outline (TO) packaging to re-orient the laser die vertically, VCSELs can be mounted in more cost-efficient packages already available to LED technology [Figure 1]. This allows VCSEL die to be handled more effectively by end customers who would prefer to develop their own packaging for small footprint VCSEL applications. However, there are additional design criteria that need to be met for VCSELs to achieve their performance targets.

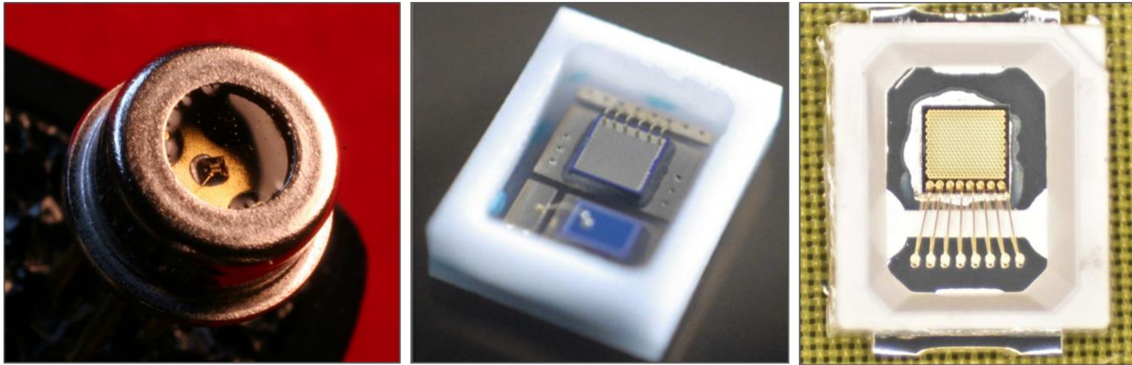

Figure 1: VCSELs integrated in TO can (left), ceramic (center), and PLCC-2 (right) packaging.

This application note goes over safe and effective handling procedures for Vixar's VCSEL die to assist with subassembly development on the customer's side. Information on the die's durability and physical characteristics are first presented. Information on die handling and attachment methods are included for those that want to package VCSEL chips. General information is provided to better assist end uses for different applications with specific requirements.

2 Die Characteristics

VCSEL die available from Vixar come in a variety of sizes. Single aperture VCSEL die for small proximity sensors are ~200 um in size while VCSEL power arrays can be almost 2 mm in length. After die fabrication, wafers are thinned to ~ 100 um in thickness before testing, dicing, and sorting into individual die.

Standard VCSEL die from Vixar are vertically conductive with the anode on the top bond pads and the cathode being the bottom substrate. A proprietary metallization stack is applied to both the top and bottom sides of the VCSEL die to reduce ohmic contact loss, improve metallization adhesion, and prevent oxidation before package assembly. A 2 µm thick layer of Au is applied as the final metallization layer to both the top (anode) and bottom (cathode) of the die for improved reliability in wire bonding, die adhesion, and thermal heat spreading.

A bond pad is integrated on top of the die for the attachment of wire bonds of 1 mil (25 µm) diameter [Figure 2]. Small VCSEL die have a bond pad region of 80-100um in width and length for a single wire bond. High power VCSELs have long bond pad regions to allow for the attachment of multiple wire bonds.

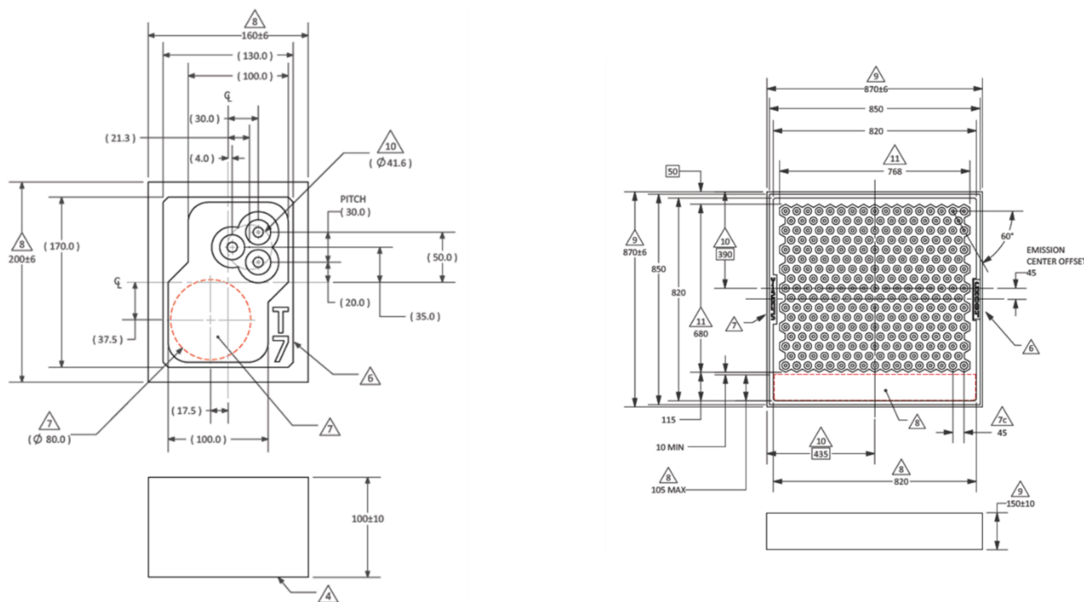

Figure 2: Example die drawings for low power (left) and high power (right) VCSELs. Wire bond pad areas are outlined in the red dashed line.

VCSEL die from Vixar are designed to be robust under standard industrial reliability standards. Vixar also conducts high temperature high humidity testing as a qualification type of test. Vixar's products are tested at 85°C and 85% relative humidity. Vixar's products are designed to reliability meet optoelectronic performance over a variety of operating conditions. Results also show that hermetic sealing is not required for VCSEL die packaging.

Reliability reports and lifetime estimates for Vixar's VCSEL die products are available on request.

3 Die Production and Delivery

Vixar VCSELs in production are 100% tested before delivery to ensure performance matches those stated in the product datasheets [Figure 3]. All VCSEL die are wafer-probed and tested for electro-optical performance. Automated Optical Inspection (AOI) is carried out to ensure products are free from chipping, cracks, and contamination. Die that fail scanning criteria are removed from delivery lots. In addition, a small sample set of die is tested from specified wafers to ensure product lots pass wafer qualification standards.

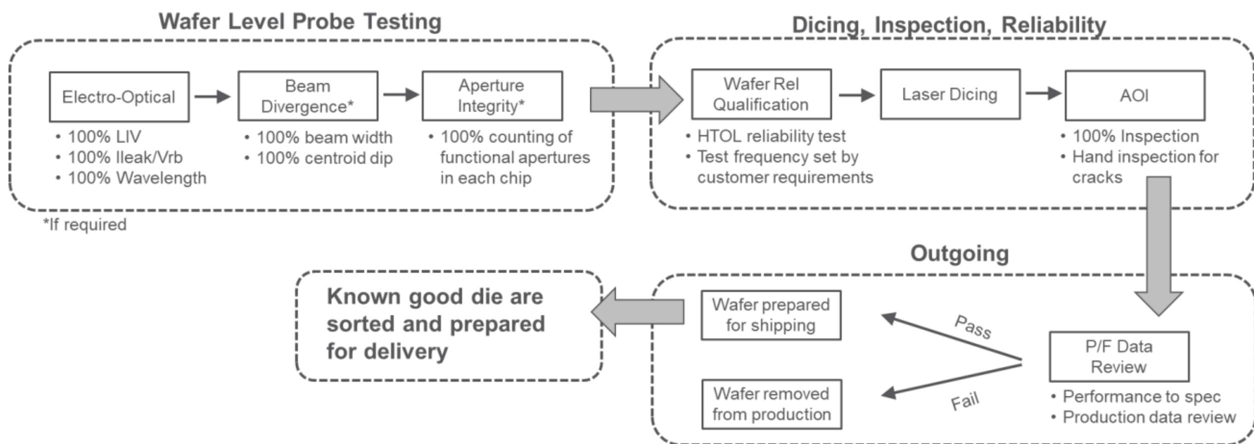

Figure 3: Production wafer test process flow for Vixar's standard die products.

Vixar offers multiple options for the shipment of its sorted die. For low volumes, die samples are shipped in 2" Gel-Paks with vacuum release technology. Sample quantities of standard die products are picked into quantities of ≤ 100 die per Gel-Pak with the use semi-automatic die sorting equipment with a die pitch of ~2mm.

For larger volumes, the preferred method of die delivery is the plastic hoop ring format with blue medium tack, non-UV tape [Figure 4]. The ring is either a 6" diameter or 8" diameter hoop ring (e.g., Perfection Products GRP-2620-4 and GRP-2620-6, respectively). Die spacing and quantity per tape is dependent on the chip size and any requirements specified by the customer. For a typical 1 mm x 1 mm VCSEL die, ~4000 die can be placed on an 8" ring with a die pitch of ~ 2 mm.

Each ring of VCSEL die is packaged inside a black conductive shipper and identified with a sticker [Figure 5], which is attached to each wafer case. The label shows product number, wafer lot number, manufacturer details, and quantity. The shipment lot is carefully arranged in a stack for multiple rings and placed into a plastic ESD bag. The sealed shipment lot must be opened in a temperature and moisture controlled clean room environment.

Figure 4: Plastic hoop ring with non-UV tape used for VCSEL die delivery (left). VCSEL die placed on Gel-Pak (right).

VIXAR Vertical Cavity Surface Emitting Laser (VCSEL) Product

Model: ___________________________

Manufacturer: VIXAR
2355 Polaris AVE N. SUITE 100
Plymouth, MN 55447 USA

Manufactured: Bare Die by VIXAR,
Fabricated or Packaged by: ___________________________________
City: ________________, Country: _________________

Wafer #: __________________
Date Code: _______________
Manufacturer Lot No.: ___________________
Quantity: ______________

Complies with FDA/CDRH 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

CDRH Accession No.: 1210159-000 Product Code: RDW

Figure 5: Product label for VCSEL die shipments.

4 Die Handling

As semiconductor devices, VCSELs are susceptible to electrical and mechanical stress that can cause immediate failure or shortened lifetime. Any mechanical handling of the top side of the die should be minimized. This is especially true for VCSELs, as damage and contamination can degrade the device's beam quality and functionality. In addition, any contact between the top surface of the die with tapes or adhesives may cause impairments such as adhesion problems during wire bonding or encapsulation.

Generally, manual handling of the VCSEL chips should be avoided, since chip damage during handling is hard to prevent. Any contact between rigid tools such as metal tweezers and the chip surface may cause irreversible damage. In cases where manual handling is needed, the ESD guideline for handling of semi-conductor devices must be observed.

Vixar die products will need die attach for the cathode and wire bonds for the anode for electrical connection [Figure 6]. All VCSEL die from Vixar are compatible with existing industrial optoelectronic chip handling methods such that conventional die picking and bonding equipment can be used. When die are processed by means of automated placement machines, care should generally be taken to ensure that an appropriate pick and place tool is used and handling specifications are adjusted to the specific die. If not calibrated, the forces applied during die pick and bonding may result in mechanical damage to the VCSEL die or unreliable die attachment. Therefore, bonding parameters should be approved by means of reliability tests.

4.1 ESD Considerations

VCSELs are electrostatic sensitive devices that can be damaged from electrostatic discharge (ESD) or electrical over stress (EOS). Single aperture VCSELs can be damaged with ESD events of < 200V (IEC61000-4-2, human body contact model) and can occur from different sources during device assembly. Operators that assemble VCSELs will not feel a discharge under several thousand volts, and VCSEL damage may occur without detection until it is in the field. ESD robustness has been observed to increase with larger VCSEL die and higher aperture count, with Vixar' power array VCSELs demonstrating intrinsic ESD tolerances over 2 kV HBM. Additional testing can classify the ESD robustness levels for each die based on the ESD models used.

Regardless of the die design, VCSEL handling requires strict precautions to minimize ESD events. The tools and operators should be ESD protected with proper garments and continuously grounded in an ESD protected area. VCSELs should be packaged in anti-static bags and stored in a clean and dry environment when not in use. If the VCSELs are hand-picked, ESD-protected tweezers at a properly equipped ESD station should be used to minimize charge buildup at the tweezer tips. For more information, please reference Vixar's application note "VCSEL ESD Characteristics and Handling Procedures."

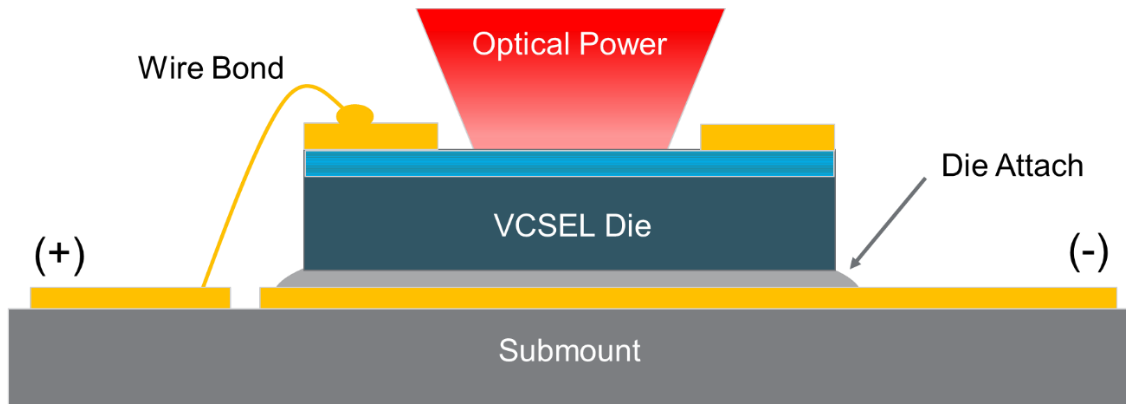

Figure 6: Drawing showing VCSEL die mounted with die attach and wire bond on a submount for both electrical and thermal conductivity.

After packaging, VCSEL die can be damaged from ESD occurrences if the corrective measures are not incorporated. For low power VCSEL die, Vixar recommends including a bi-directional ESD protection diode in parallel with the VCSEL to protect the laser diode against ESD events. Please note that the addition of an ESD diode may degrade the product's performance during high-speed (>1 GHz), short pulse width operation. In addition, die placement on a PCB should be protected with additional electronics for any EOS factors that may occur while the device is in the field.

4.2 Die Attach

Die attach methods must consider performance and environmental factors to ensure the VCSEL performs as expected at a reasonable cost. The main purpose for die attach is electrical and thermal conductivity between the VCSEL die and the bonding substrate. However, die attach materials with higher thermal conductivity and bond robustness typically are more expensive and may require unconventional production equipment. In addition, some die attach materials are not compatible if additional processing requires secondary reflow after die bonding.

For low power (< 50 mW) VCSELs, conductive silver-based epoxy is preferred as the die attach material. Conductive epoxy is a cost-efficient method that is compatible with most die assembly lines, as the material is easily dispensed and cured at low (< 200° C) temperatures. While the thermal conductivity is low (typically < 10 W/mK), the performance of low power VCSELs isn't significantly affected due to die's relatively high internal thermal resistance. Vixar's single aperture die have been qualified for die attachment processes using silver filled conductive epoxies or adhesives.

High power VCSEL die have significantly higher optical power and thus need improved thermally conductive die attach material to ensure high performance after packaging. Pressure-less sintered silver is recommended for high power VCSEL applications, and it is easily dispensed and cured at moderate (~ 200° C) temperatures. The final die attach with sintered silver results in thermal conductivity levels > 100 W/mK.

Additional die attach methods can also be considered for die attachment based on end use concerns. Eutectic AuSn solder is one of the most used attach materials for high power laser diode applications due to its high conductivity (>50 W/mK), high corrosion resistance, and high yield strength. However, this fluxless solder needs to be applied through nontraditional methods and requires high melting temperatures (~ 280° C) for solder reflow. Due to the additional manufacturing complexity, AuSn is typically not recommended for VCSEL die attachment unless high environmental resistance is necessary.

Silver epoxy, sintered silver, and AuSn solder are all compatible with secondary solder reflow processes. Unlike traditional solder, these materials will not liquify at traditional solder reflowing temperatures (~260° C) to ensure the die does not move during any additional processing.

In order to guarantee the best thermal and electric characteristics, it should be ensured that the die attach material is optimally dispensed to cover the VCSEL cathode. Underfilling will result in voids that degrade VCSEL performance and bond reliability, and overfilling will lead to silver migration that may create an electrical short across the VCSEL's anode (top) and cathode (bottom). The bonding force is also critical in order to avoid excessive squeeze out of die attach material. Thus, the appropriate bonding force depends on the specific die attach method and thus needs to be adjusted carefully to develop an optimal bond line thickness between substrate and VCSEL die.

For more technical information and recommendations on die attach materials, dispensing procedures, and recommended bonding forces, please contact your supplier.

4.3 Wire Bonding

For the wire termination, Vixar recommends a standard gold ball wire bonding process for all VCSEL die products. A correct bonded ball size is essential for robust attachment to the wire bond pad on the die. Vixar's die products are designed with wire bond pads that accept bonding from 1 mil (25 µm) diameter gold wiring. All wire bonds or any metallic bond connections shall be within the designated bonding area on the VCSEL die. Wire bonds outside of this region can damage the active VCSELs or the nitride passivation layer at the edge of the die. Thus, off-pad bonding during the process must be avoided.

Single aperture VCSELs only require a single wire bond to deliver sufficient current. For high power VCSEL die, a higher quantity of wire bonds are needed to withstand the expected driving conditions [Figure 7]. Insufficient wire bonds will result in wire fusing and catastrophic failure of the device. The maximum DC current a standard 1 mil gold wire bond can handle is 0.7 Amps. For example, if a high power VCSEL die is driven with an expected DC forward current of 5 Amps, at least 8 wire bonds should be used per die to distribute the forward current.

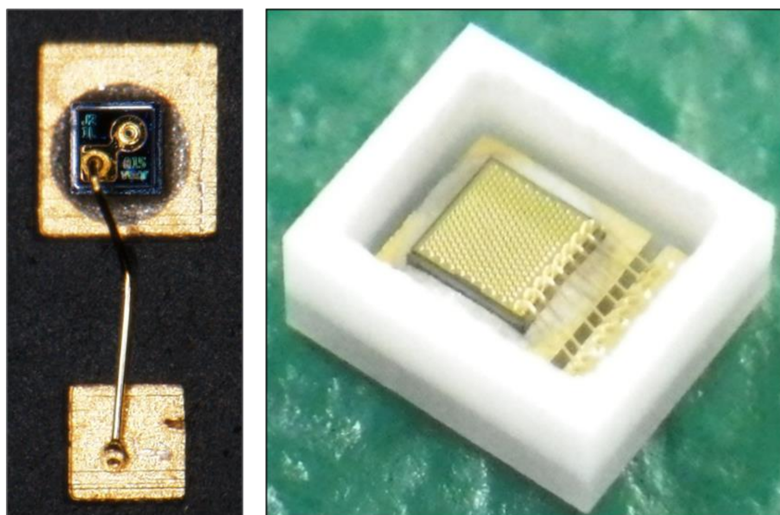

Figure 7: Single aperture VCSELs only require one wire bond (left). A power array VCSEL rated for 5 amps requires 8 wire bonds (right).

VCSELs driven under pulsed conditions may be able to handle higher forward currents in comparison to DC operation. Unfortunately, there is no simple rule that calculates the minimum wire bonds required as fusing is dependent on pulse current, pulse width, and duty cycle. For example, pulsing conditions with high duty cycles may not allow sufficient time for thermal dissipation between individual pulses, resulting in delayed fusing. If the pulse width is sufficiently long enough (>1 ms), then it's best to utilize DC current rules when determining the minimum wire bonds required.

Wire bonding equipment must be properly tuned to ensure adequate wire bond strength while minimizing damage to the VCSEL die. Excessive wire bonding forces induced by the tool to the surrounding material can cause shunting leakage and/or junction damage. Due to the large number of manufacturers of wire bonding equipment and the multitudes of capillary designs, it is difficult to give a universally valid guideline for process parameters on wire bonding.

For further information on wire bonding, capillary tools, or for recommendations on designs, please contact your supplier.

4.4 Encapsulation

Die and package encapsulation is a popular method for low power optoelectronic components to protect the die and the wire bonds from any mechanical damage during secondary packaging steps and in the field. Guidelines for choosing an encapsulation material is dependent on the desired thermal stability, transmission performance, gas/humidity permeability, and refractive index match with the VCSEL die. The selection of an appropriate casting compound should consider the fact that it doesn't contain any corrosive chemicals or components and that no corrosive compounds are produced which might result in damage to encapsulated VCSEL die.

Materials used for optoelectronic devices include epoxy, silicones, and hybrid materials which combine the strengths of both materials. Epoxy materials are used for most VCSEL packaging due to its ease in packaging and gas impermeability. While silicones exhibit intrinsic high thermal and radiation stabilities, their permeability to gases make them more susceptible to corrosive environments and humidity-based "popcorning" effects during solder reflow or thermal shock.

In addition, encapsulation selection needs to consider the expected temperature range the product may experience. At elevated temperatures, the encapsulation material will expand at a greater rate than the VCSEL die. Delamination may occur between the encapsulation and the die. Material expansion may also cause die or ball lift-off, resulting in an open circuit and catastrophic failure of the device. While cold temperatures are typically not an issue, extreme cases can cause encapsulation cracking in materials with high glass-transition temperatures.

Unlike LEDs, die encapsulant can impact the optical performance of the VCSEL die, as the material's refractive index will affect the overall performance of the VCSEL. The VCSELs in Vixar's standard portfolio are designed to work optimally in open air ($n \sim 1$). Standard encapsulations have refractive index values of $n \sim 1.5$ and shift the DBR's reflectivity and resonance inside the VCSEL. Typically, encapsulants have been observed to reduce the efficiency of these VCSELs by ~10%. While this is of minor concern for low power VCSELs, the encapsulation of high power VCSEL die should be avoided due to efficiency and thermal degradation concerns inside the laser diode. Protecting high power VCSELs with a cover glass window with an AR coating is the preferred alternative to encapsulation which protects the VCSEL from mechanical damage while not impacting the laser diode efficiency.

5 Single Spectral Mode VCSELs

Vixar offers two die products, 795 nm and 895 nm SM VCSELs, that are designed for atomic-scale clocks and magnetometers. The diameter of these single aperture VCSELs is significantly reduced and integrated with a surface grating, so the active transverse mode is the fundamental mode with a well-defined polarization of the light. These devices are known as single spectral mode (SM) VCSELs that exhibit a polarized Gaussian output, high spectral purity, and low angular divergence. Wafer probe test data allows Vixar to sort each VCSEL into "bins" of operating wavelength at a pre-specified operating temperature. The wavelength range within each bin is ± 0.5 nm.

Additional care is required to maintain SM functionality for these products. Most die attach materials and methods will affect the performance of the VCSEL die, including the operating wavelength and polarization. Vixar recommends using silver epoxy cured at 85°C for 3 hours when curing 795 nm and 895 nm die. Higher temperatures and/or faster cure times induce stresses that will affect the polarization and wavelength. Die encapsulation will negate the effect of the VCSEL's surface grating and is not recommended.

6 Conclusions

Vixar strives to deliver high quality products that are consistent with customer expectations. Regardless, the method of VCSEL packaging may impact its electrical and optical performance both initially and over its lifetime. Understanding the physical and optical properties of the VCSEL die helps guarantee that the laser diode will function as expected over the application's lifetime after die handling and assembly.

Knowing the various end-case designs involving laser diode integration, VCSEL die are designed for both high performance and high packaging reliability with traditional optoelectronic die assembly processes. To assist customers in laser integration, recommendations on VCSEL die packaging are laid out laser packaging including die picking, die attach, and wire bonding specifications. These recommendations ensure anticipated optical output power, adequate thermal dissipation, and sufficient mechanical robustness for the end application.

For more information on packaging VCSEL die, please contact Vixar at Sales@Vixarinc.com.