Vixar Application Note

VCSEL Thermal Performance

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1 Executive Summary

Vixar has developed a package that contains a high-power vertical cavity surface emitting laser (VCSEL) array. This package can also support a photo detecting diode. This device is primarily used for sensing distance by use of time-of-flight sensing. A VCSEL array typically runs at 1-4 watts of power in a package footprint often less than 4 mm x 3 mm. Thermal management is critical to ensure the desired lifetime of the VCSEL device. This application note will provide information regarding thermal management of these packaged devices.

2 Package Structure

The Vixar package consists of a VCSEL die (2 watt and 281 apertures) attached to a gold-plated copper pad (as shown in Figure 1). This pad is connected through vias to a cathode pad on the bottom of the substrate. The substrate is 0.5 mm thick aluminum nitride.

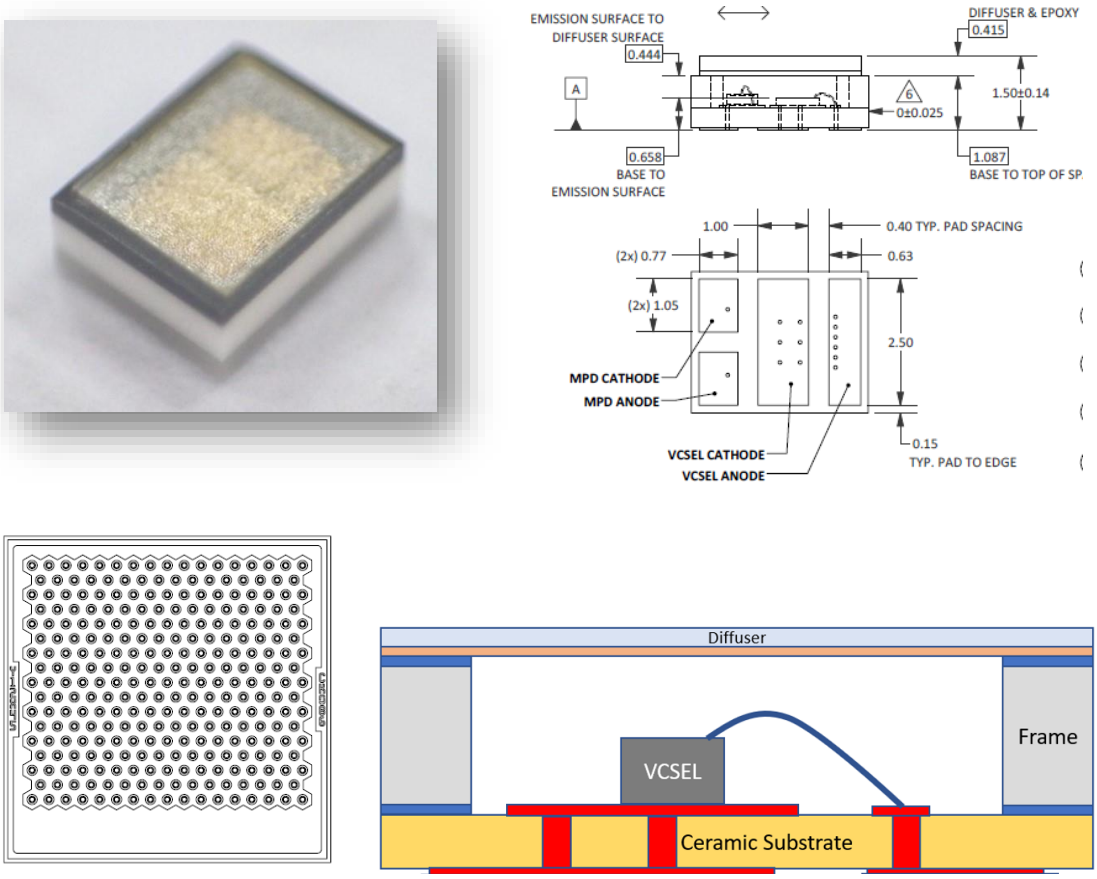

Figure 1. An example of a Vixar VCSEL array package design and a 2W power array.

3 Thermal Path

Heat is generated in the active region of the VCSEL near the die surface. This heat must be dissipated through the bottom of the die, through the package body, and through the printed circuit board (PCB) to the external ambient environment. The path of this heat dissipation is illustrated in Figure 2. The efficiency of this heat flow to the solder joints is dictated by the thermal conductivity of the package materials. Heat flow from the solder joints to the external ambient environment is dictated by the design of the PCB and any cooling system created by the application designer. This application note will demonstrate how to calculate these important thermal values to prevent overheating of the VCSEL device.

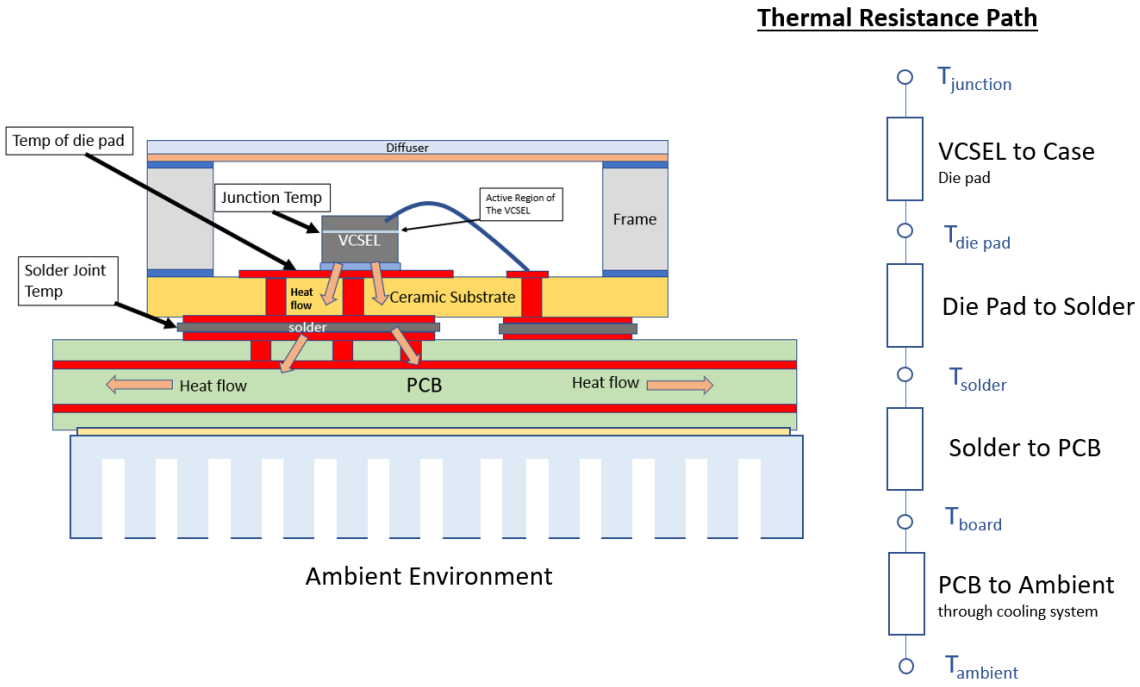

Figure 2. Thermal resistance path from the VCSEL to the external ambient environment.

4 Package Thermal Resistance

The Vixar package was designed for optimal thermal management. Table 1 shows the thermal conductivity values for critical elements of the package. For example, commonly used epoxy die-attach materials have thermal conductivity values near 30 W/m-K. However, this package uses a sintered silver paste that consists of a high density of silver particles bonded together for excellent thermal and electrical conduction (a cross section is shown in Figure 3). The thermal conductivity of this sintered silver paste is greater than 200 W/m-K. This enables heat to pass

easily from the die through the die-attach material to the copper die pad. This heat then passes through the aluminum nitride at the base of the package to the solder joint. From here, it is the role of the circuit board to move the heat efficiently to the exterior ambient environment. This is often accomplished using thermal vias to route heat to copper planes in the board.

Table 1. Thermal conductivity of critical materials

Component	Material	Thermal Conductivity
VCSEL Die	GaAs	70 W/m-K
Die Attach Material	Sintered Silver Paste	200 W/m-K
Die Pad Material	Copper	385 W/m-K
Base of the Package	Aluminum Nitride	170 W/m-K
PCB Laminate	FR4 Epoxy	0.3 W/m-K

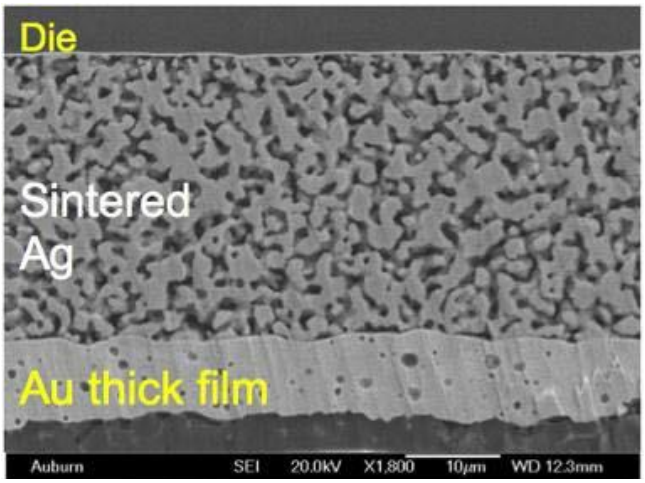

Figure 3. An example cross section showing sintered silver die attach material.

5 Thermal Calculations – Junction Temperature to Die Pad

Heat is generated in the active region of the VCSEL from Joule heating due to current flow. The junction temperature (temperature in the active region of the VCSEL), can be calculated by determining the power running through the device minus the power being dissipated through release of photons (the emission). For example, the junction temperature to die pad can be calculated by the equation:

$$T_j - T_{\text{die pad}} = Rth * (I_o * V_o - P)$$

Where:
- I_o = The operating current flowing through the VCSEL
- V_o = The voltage at operating conditions
- P = The optical power emitted.
- R_{th} = The thermal resistance of the VCSEL (°C/mW)

The thermal resistance (R_{th}) is a measure of how much the VCSEL epitaxy resists the flow of heat. Two quantities are required to determine R_{th}, the VCSEL wavelength temperature coefficient (R_λ) and the dissipated power as a function of wavelength (R_{diss}).

$$\mathbf{R_{th} = 1 / (R_\lambda * R_{diss})}$$

The wavelength temperature coefficient is a well characterized physical value, determined by the VCSEL lasing wavelength, and is primarily independent of the VCSEL epitaxial design and aperture size. For 940 nm, R_λ is 0.066 nm/°C and for 850 nm R_λ is 0.059 nm/°C.

To determine R_{diss}, the optical emission from a single aperture is measured as a function of drive current. Any change in the VCSEL wavelength is due to a change in temperature caused by Joule heating of the VCSEL junction (the temperature at the base of the die is held constant). The peak wavelength of the fundamental mode is recorded for each of these currents (see Fig. 4 left). R_{diss} is the slope of the power vs. wavelength plot and has units of mW/nm (in the case shown in Figure 4, R_{diss} is 2239 mW/nm for an 850 nm device and 1861 mW/nm for a 940nm device). The thermal resistance for this 2-watt array is then calculated to be 0.0075 °C/mW for an 850 nm device and 0.0082°C/mW for a 940nm device.

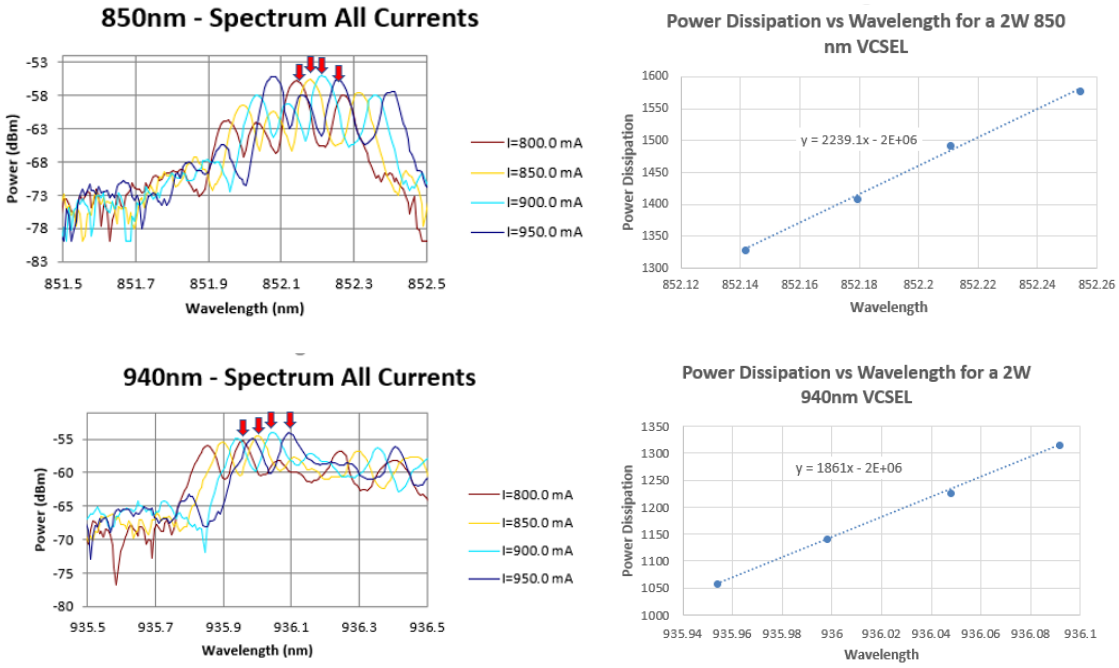

Figure 4. Wavelength shift at different operating currents and the resulting power dissipation vs. wavelength plot.

With an R_{th} value of 0.0082 °C/mW or **8.2 °C/W**, we can now determine the junction temperature to die pad at 940nm VCSEL operating conditions. The emission curve of a 940nm 2W device is shown in Figure 5. To achieve 2000 mW of emission it requires 2.2 volts and 2800 mA of current. This means 4.16 watts of power is being dissipated as heating. The junction temperature to die pad calculation then gives a result of:

$$T_j - T\text{die pad} = 34°C$$

6 Junction Temperature from Die Pad to Solder Joint

Due to the high thermal conductivity of the materials used in this package, thermal resistance between the die pad and the solder joint is quite low. The heat flow through the bottom of the package is dominated by the aluminum nitride substrate which is 0.5 mm thick. If we assume an area of 2 x 3 mm the thermal resistance of the package base is calculated by (refer to appendix A):

The Substrate Thickness/(Area x 170 W/m-K) =

0.0005m/(0.002m x 0.003m x 170 W/m-K) = 0.5 K/W.

A device that emits 2 watts of light must dissipate 4.16 watts of power. Therefore, the expected temperature differential between the die pad and the solder joint is 2 °C. This gives a total junction to solder joint temperature of 8.2 + 0.5 = 8.7 °C/W (or 36 °C in this case). It then becomes important for the design of the PCB to pull the heat away from the solder joint region. If this is not effective, the junction temperature of the die could become too high. The following sections will address the question, what temperature is too high for a VCSEL?

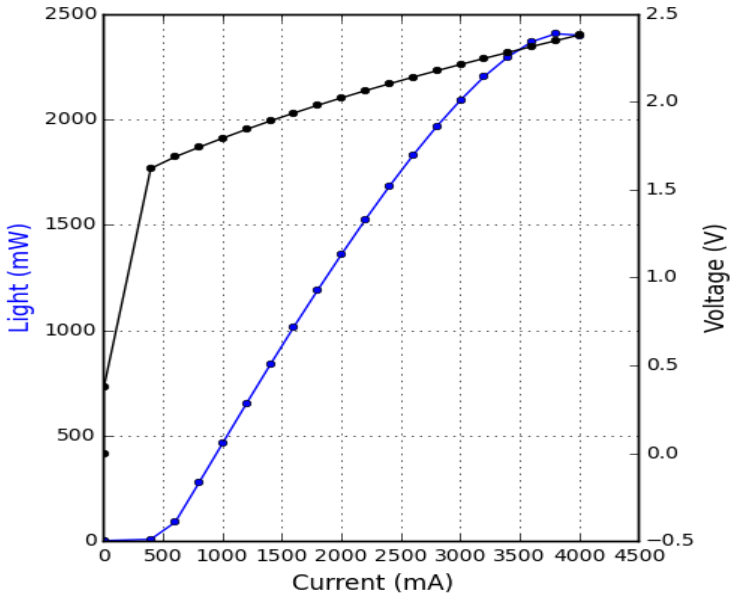

Figure 5. The emission plot for a 2 watt, 940nm VCSEL device.

7 Duty Cycle Calculations

The calculation for junction temperature used above assumed a constant width (CW) current which is a worst-case situation. These power array VCSEL devices are often used in pulse mode with duty cycles of 10% or less. For short pulse widths of less than 10 microseconds the junction temperature does not likely reach the value calculated in CW mode. For longer pulse widths the CW temperature may be reached, but only for short duration and the device can cool down between pulses. If the duty cycle is 10%, then only 10% of the CW calculated power

needs to be dissipated. In this situation where 4 watts of power is dissipated by the die at CW conditions, then 0.4 watts would need to be dissipated at 10% duty cycle. This reduced power in pulse mode makes it more manageable for the system designer to draw the heat away from the solder joints to keep the solder joint temperature at a safe level.

8 Maximum Operating Temperature of a VCSEL

A VCSEL has three operating regions as shown in Figure 6. At lower current levels the emission increases with current in a nearly linear fashion. Operating in this region allows reliable life predictions because the failure mode is well understood, and acceleration factors are known. At some point rollover occurs and the emission degrades with increasing current. It is undesirable to operate in this region due to poor efficiency and increased degradation of the VCSEL faster than known acceleration factor would suggest. Eventually a point is reached where the junction temperature is so high that emission ceases all together.

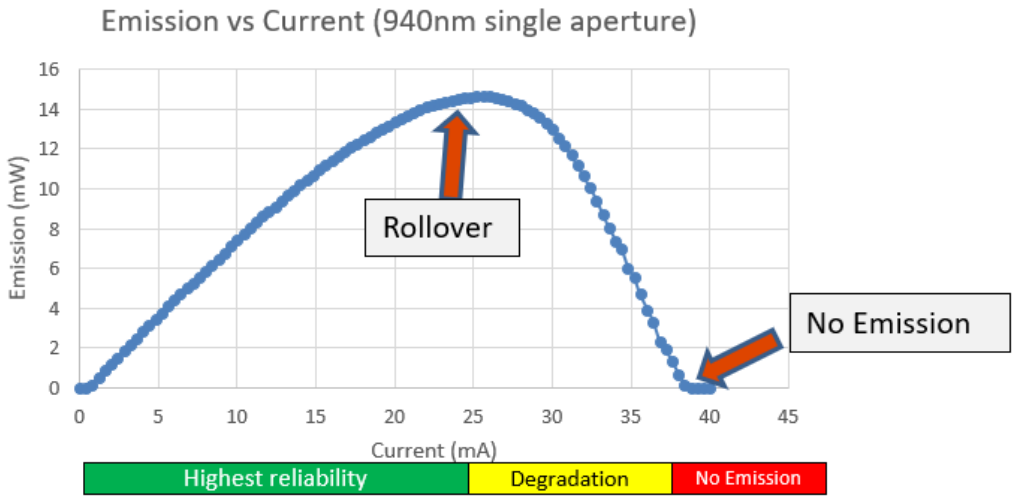

Figure 6. Behavior of a single aperture VCSEL at increasing CW current. Degradation begins at rollover and eventually leads to no emission.

Emission curves for a 2W device mounted in a Vixar package are shown in Figure 7. The rollover point occurs is just over 6000 mA of current and 3000 mW of emission power. The maximum junction temperature at rollover is calculated to be:

25°C + [(2.4V * 6000mA – 3300mW) * 0.0082 °C/mW]

= <u>116 °C</u>

If we assume a long pulse width of greater than 10 µsec where the CW junction temperature increase of 36°C is reached, this means the solder joint temperature should be kept below 80°C (at 2 watts of output and 4 watts of power being dissipated). Higher temperature is allowed but may result in reduced emission over the length of the pulse.

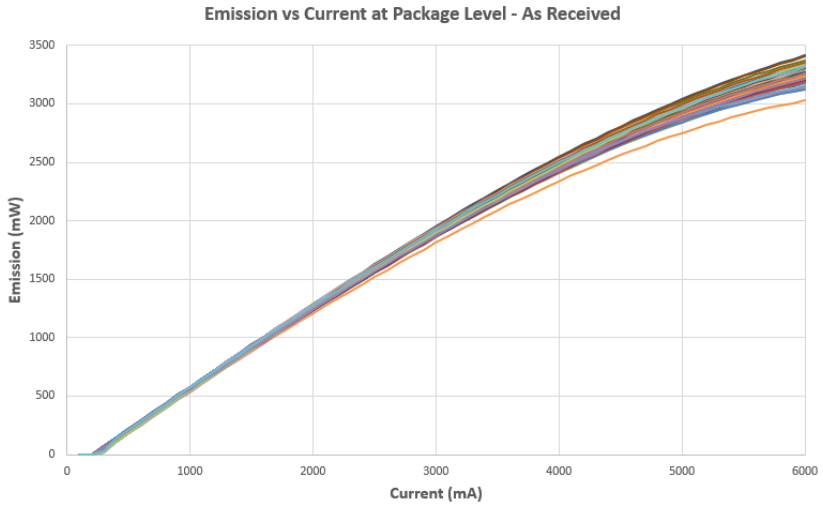

Figure 7. Emission curves for 71 VCSEL devices (2W 940 nm) in a Vixar package.

If the duty cycle is 10%, the required power dissipation for the board is 10% of the CW power. So instead of 4 watts of power being dissipated it is only 0.4 watts. If we assume an ambient temperature of 40°C, this would allow a thermal resistance of the board to ambient temperature to be:

(80C – 40C)/0.4 W = 100 °C/W

Higher ambient temperatures would require a more thermally efficient board design. The resulting thermal resistance path values are shown in Figure 8.

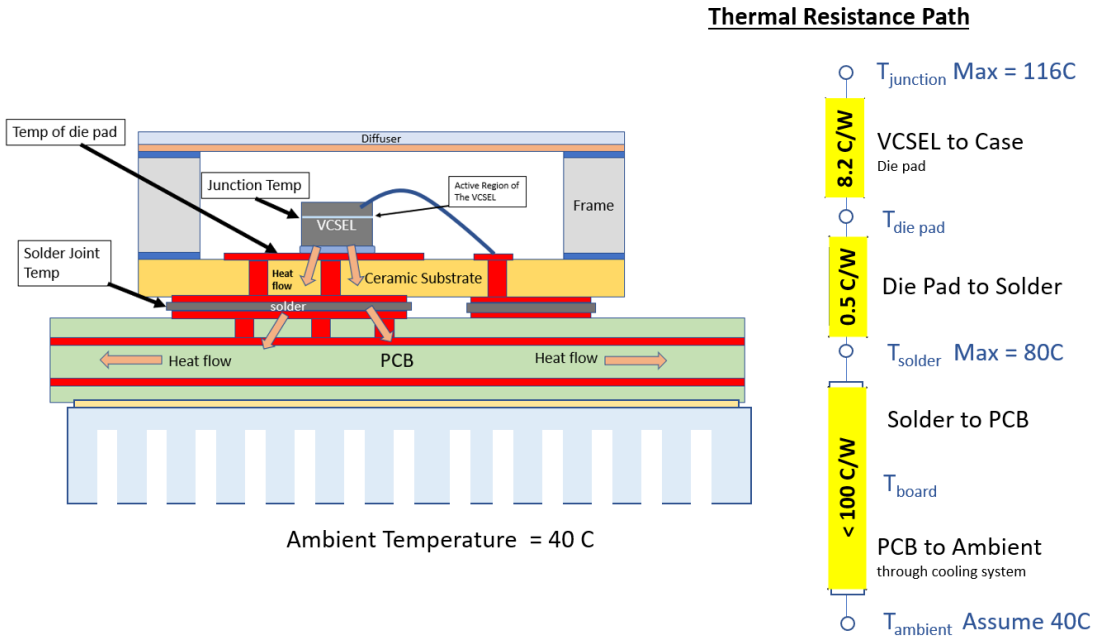

Figure 8. Thermal resistance values calculated for a 2W power array VCSEL in a Vixar package.

9 Conclusion

Vixar has designed a thermally efficient package structure for power array VCSEL devices. We calculate a junction to die pad temperature increase of 8.7 °C/W of dissipated power. The maximum advisable junction temperature of the VCSEL is 116°C. Therefore, the solder joint temperature should not exceed 80°C while operating the device. If the ambient air temperature is 40°C and the duty cycle of the device is 10%, the system supporting the VCSEL should have a thermal resistance of less than 100 °C/W. This application note demonstrated the calculations used to determine the thermal requirements of the board depending on the use conditions of the VCSEL device. The system architect can therefore design the boards cooling capability accordingly.

10 Appendix: Definitions of Thermal Conductivity and Resistance

Thermal Conductivity

For the case of one-dimensional heat-flow (which is assumed to prevail for the purposes of this document), thermal conductivity (k) is defined as follows (Fourier's Law:)

EQUATION 1:
$$k = \frac{q \cdot t}{A \cdot \Delta T}$$

where: q = heat flow (or power) in Watts
t = length of heat path (i.e., interface thickness) in meters
A = area in meters
ΔT = temperature difference across the interface, in degree C

(Thermal conductivity is often expressed in reduced units of W/mK or "Watts per meter-Kelvin")

It is important to remember that thermal conductivity is a material (i.e., "bulk" or "intrinsic") property and does not depend on the geometry of the test assembly. It simply describes the ability of a given material to transfer heat through internal heat conduction. Most critically, it does not account for any interfacial effects that may impede heat-flow, often to a significant degree.

Thermal Resistance and Thermal Impedance

Thermal resistance (R) is an empirical property derived from the often-used (though sometimes misleading) analogy between electrical and thermal conduction:

EQUATION 2:
$$R = \frac{T_1 - T_2}{q} = \frac{\Delta T}{q}$$

where: T_1 =component temperature
T_2 = heat-sink temperature

(Thermal resistance is commonly expressed in units of °C/W or "degree-C per Watt")

Thermal impedance (Z) is defined as the temperature gradient per unit of heat flux, (q / A), passing through the interface. It is calculated by simply multiplying thermal resistance by the component area:

EQUATION 3:
$$Z = \frac{\Delta T}{\left(\frac{q}{A}\right)} = R \cdot A$$

(Thermal impedance is expressed in units of °C-in²/W – "degree-C inch squared per Watt" or °C-cm²/W – "degree-C centimeter squared per Watt")

Thermal resistance and thermal impedance are not material properties and should be determined individually for each component/heat-sink configuration. In contrast to

Ref: 3M Technical Bulletin, http://multimedia.3m.com/mws/media/122268O/characteristics-of-thermal-interface-materials.pdf