Vixar Application Note

VCSEL EOS/ESD Considerations

Contents

1 Introduction

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) are related types of overstress events at opposite ends of a continuum of power/time stress conditions. EOS is used to describe the thermal damage that may occur when an electronic device is subjected to a current or voltage that is beyond the specification limits of the device over a long duration (generally >1 ms). ESD is the sudden release of static electricity when two objects come into contact resulting in a high voltage, moderate current event that occurs in a short time frame (generally <1 us).

Both events are known, well documented, and constant threats to the life of most semiconductor devices. While ESD is often considered a subset of EOS, it can be difficult to differentiate the damage caused between these two types of events. The same features that give Vertical Cavity Surfaced Emitting Laser (VCSEL) devices their unique properties, such as inherent fast response time and small size, also make them more susceptible to ESD and EOS events.

2 VCSEL ESD Susceptibility and Protection

Depending upon device design VCSEL devices can be susceptible to ESD damage at threshold voltages ranging from less than 100 V (for very small devices) to over 1000V (typically for larger devices) under Human Body Model (HBM) test conditions. These voltage levels are lower than many other semiconductor and optoelectronic products and puts some VCSELs in the most ESD sensitive classes for electronics. The active area of a VCSEL is significantly smaller than that of an edge-emitting laser, so the ESD susceptibility is greater for the VCSEL [1]. An ESD voltage of 100 V is far below the 2000 V minimum that is perceived by a person, so a device could be damaged without the event ever being observed.

Industry research has shown that the main variable which affects the susceptibility of VCSELs to ESD is the aperture size. As the aperture diameter decreases, the current density or localized energy of an EOS/ESD event increases. Figure 1 displays ESD susceptibility/voltage vs. aperture size for VCSEL devices from Vixar, Honeywell, and Agilent [2].

As can be seen from Figure 1, Vixar's S and Q single mode die are highly susceptible to ESD damage. Therefore, Vixar recommends an ESD protection diode be added to the packaged component. Vixar can include a bi-directional back-to-back ESD protection diode that protects VCSELs against ESD events of 1KV or higher. Since the ESD diode has a capacitance of approximately 80 pF, it will limit the modulation frequency of the VCSEL package to 35 MHz or less. Thus, an ESD diode is impractical for high modulation applications.

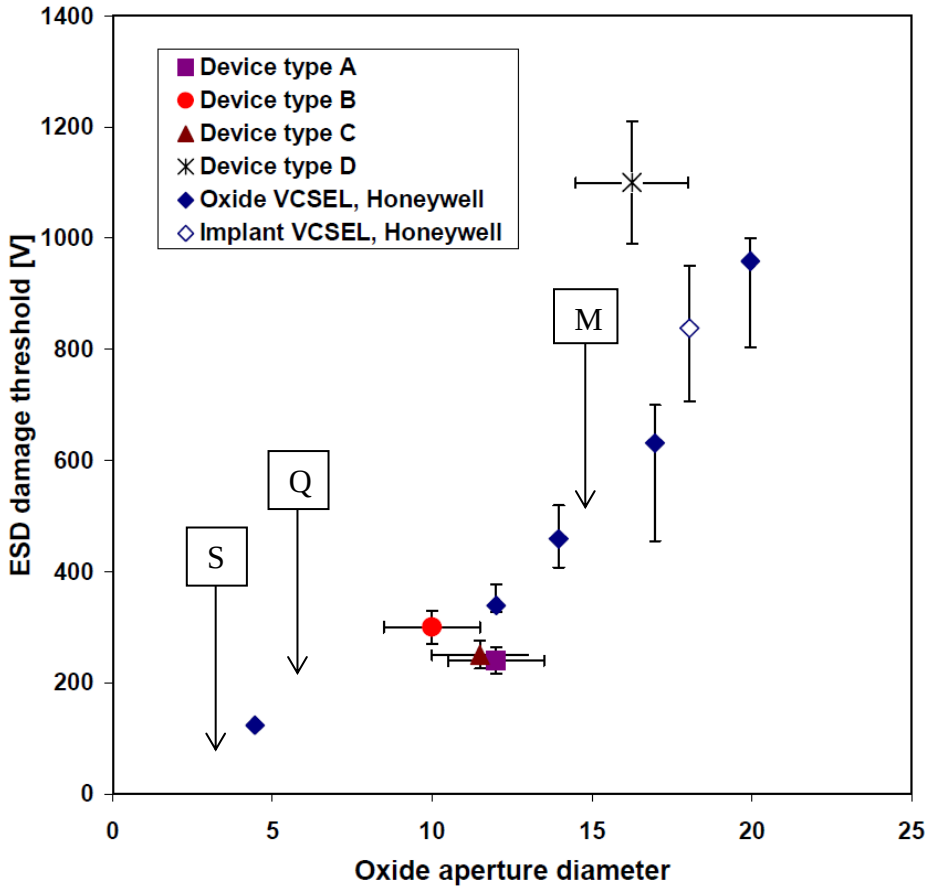

Figure 1: ESD voltage thresholds for oxide VCSELS (Human Body Model, reverse bias) [2]

3 ESD Control

ESD events can be avoided by following industry standard guidelines such as ANSI/ESD S20.20. The guideline explains how grounding, safe package handling, air ionizers, and many other precautions can be put into place to minimize ESD events. This procedure only applies to the Human Body Model (HBM) events larger than 100 V. For VCSEL products, further precautions such as floor grounding, widespread ionizer usage, and more stringent ESD technical requirements and more frequent verification may be required.

4 EOS Control and Precautions

EOS precautions also need to be taken when working with VCSELS. The following is a list of examples of how EOS events can inadvertently occur.

- Connecting the VCSEL device to a power supply that is already on. This can release a rush of unwanted current into the device from a charged open circuit.
- Intermittent connects from the VCSEL to the power source. This can be caused by pins that are too short for a socket or mismatched in length to all fit well into a socket.
- Turning on a power supply already set to a voltage or current using the AC main switch. A large voltage/current spike can be propagated to the device when the instrument is first turned on. Vixar recommends setting the power supply to 0 V, turning it on, and then slowly adjusting it to the desired current.
- Reverse biasing the VCSEL should be avoided. Accidently setting the current source instrument to the wrong polarity could damage the device. Currents greater than 0.1 μA and voltages greater than 5 V in reverse bias have been shown to cause damage.
- Setting the VCSEL power source to force voltage instead of current. If the voltage is too high, even in the forward bias direction, the generated large current will damage the device. The current limit should be set just above the desired operating current.

In general, use gradual turn-on conditions when driving the VCSEL in the forward bias direction using a current source and avoid reverse bias currents of any kind.

5 Identifying EOS/ESD Damage

Sufficiently large ESD/EOS events may cause immediate symptoms such as lowered output power, dark areas within the emission aperture, and large reverse leakage. Lower level EOS/ESD events by contrast may cause no immediate effects but can introduce one or more crystal dislocations that can grow into dark line defects over time. The device may not fail for minutes, hours, days, weeks, or longer after the stress event, but the device's reliability will have been compromised. Because of this, it can be very difficult to determine the root cause or exactly when and where the stress event occurred.

A sufficiently large EOS/ESD event can usually be easily identified because of physical damage observed at the surface of the VCSEL. The physical damage can be identified by melted pad or bonding metal, discoloration at the surface, or other changes to the VCSEL structure. Damage can also sometimes be observed by biasing the device with current below the lasing threshold and observing the emission from the aperture. Dark regions in the emission pattern, especially around the outside of the device aperture, can indicate EOS/ESD. An example emission pattern of an ESD damaged VCSEL can be seen in Figure 2. The dark areas on the outside left and right sides of the aperture in Figure 2 are typical signs of ESD damage.

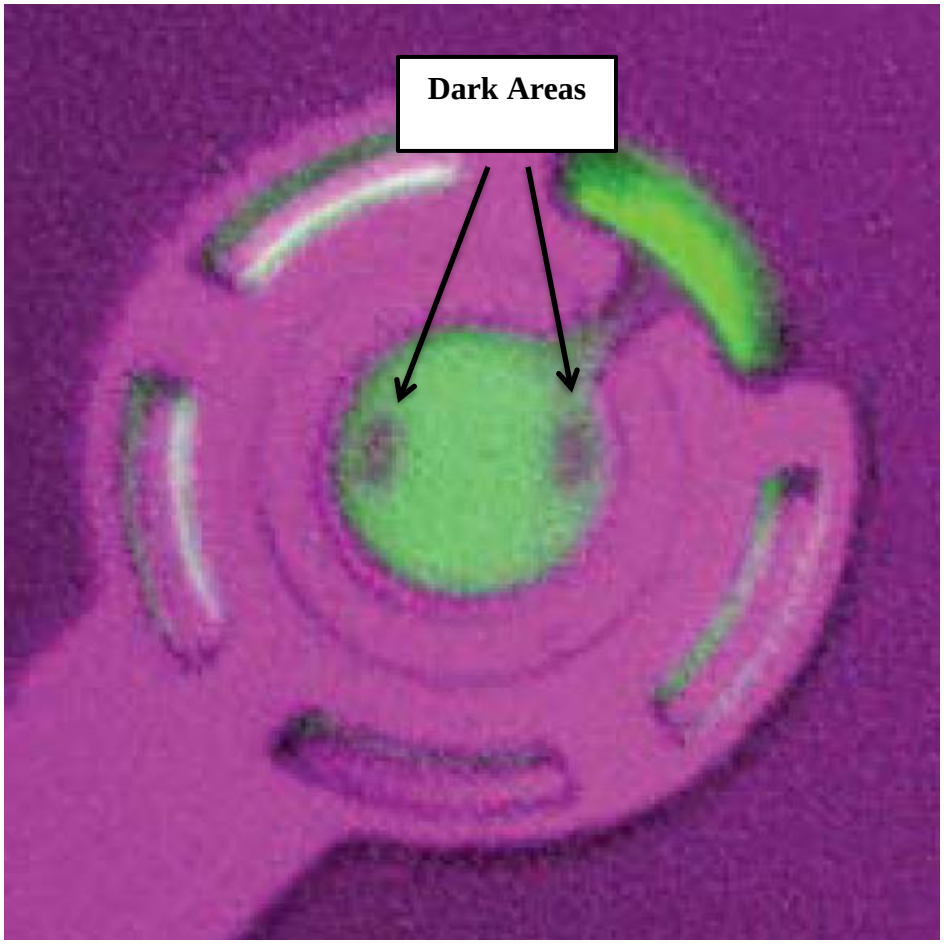

Figure 2: VCSEL emission of an ESD damaged device [4]

In many instances, EOS/ESD damage cannot be visibly observed at the surface of the VCSEL, but there are electrical signatures that do indicate EOS/ESD damage. ESD and EOS are detected electrically using a reverse bias leakage test. The reverse current for a damaged VCSEL is much higher for a given reverse voltage. Figure 3 shows the effects on a VCSEL's reverse leakage current when damaged or zapped by ESD. While the reverse bias leakage test can also indicate other types of defects, it is not usually an indicator for intrinsic VCSEL wear out.

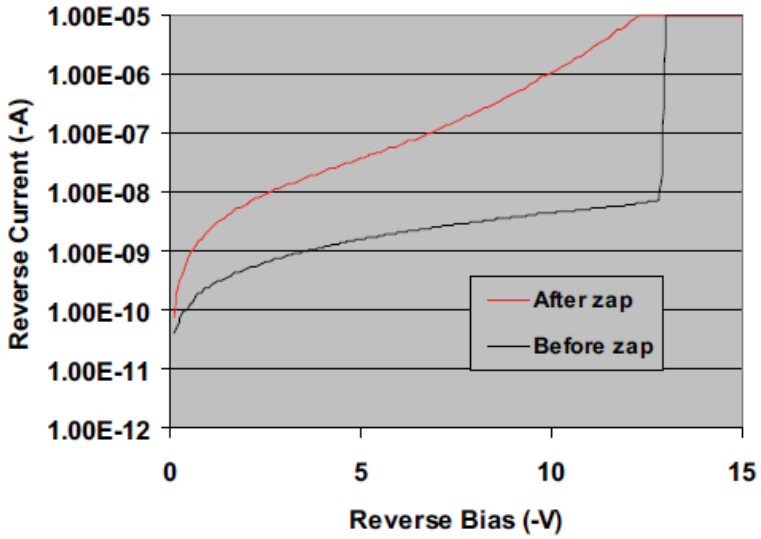

Figure 3: Typical reverse bias characteristics of an ESD damaged VCSEL [4]

Vixar recommends that customers do not attempt reverse leakage measurements. Great care needs to be taken when performing a reverse leakage measurement. The act of doing the measurement can damage the device if proper instrumentation precautions are not taken. For instance, when forcing voltage in the reverse direction, the current compliance/limit should be set to a value of 0.1 µA or lower on the instrument being used.

The forward voltage output power (L), Current (I), Voltage (V) curves (i.e., LIV curves) for a VCSEL are not typically good indicators of EOS/ESD damage. For moderate to high levels of EOS/ESD damage, the slope efficiency and threshold current may be quantitatively observable. However, latent damage for low levels of EOS/ESD can occur which may not be immediately observed in the forward bias measurements. Damage may only appear after 10s to 1000s of hours of operation afterwards. Therefore, Vixar finds the reverse bias measurements to be a more sensitive measure of whether EOS/ESD damage has occurred.

6 EOS/ESD Screening

At Vixar screening techniques are used at multiple levels of assembly to identify defective VCSELs, including those possibly damaged by EOS/ESD, and eliminate them from the population. The tests include but are not limited to:

- Over 24 hours of burn-in, excluding unpackaged, bare die sent directly to the customer.
- Electrical characterization both in the forward and reverse biased direction.
- Optical power characterization.
- Optical microscopy inspection for physical defects

7 Enhancing VCSEL Lifetime

Even a perfectly fabricated, packaged, and operated VCSEL containing no EOS/ESD damage or defects will eventually wear out. The lifetime of a VCSEL is very dependent on the operating temperature and current used. The lifetime can vary greatly, even by many years, for the same design using even slightly different operating conditions. For a small aperture device, such as a single-mode VCSEL, decreasing the operating temperature from 40° C to 30° C can double the lifetime. For the same design decreasing the operating current from 2 mA to 1 mA can increase the lifetime by over six times. The current applied to the VCSEL can also cause a secondary effect on the lifetime of the VCSEL by increasing the VCSEL's junction temperature. If the VCSEL is used in a pulsed application, where the VCSEL is only on for a short portion of the cycle, then this junction heating affect can be significantly reduced. Since the VCSEL is only on for a fraction of the cycle, its actual usage time will be diminished by that same percentage.

8 Conclusion

Vixar highly recommends using stringent ESD and EOS safety procedures when handling VCSEL devices due to their inherent sensitivity. Vixar also recommends that an added ESD protection diode be considered for our small aperture devices. For applications where the added ESD diode protection is not feasible, extra ESD precautions should be taken in consideration. ESD precautions help improve the reliability of VCSEL devices. The long term reliability of the VCSELs is also affected mainly by the operating conditions under which the devices are used. Both VCSEL temperature and forward current should be minimized to increase the device lifetime.

9 Reference

[1] T. Kim et al, "Degradation Behavior of 850 nm AlGaAs/GaAs Oxide VCSELs Suffered from Electrostatic Discharge," *ETRI Journal*, Volume 30, Number 6, December 2008

[2] J. Krueger et al, "Studies of ESD-related failure patterns of Agilent oxide VCSELs," Proc. SPIE, Volume 4994, 2003, pp. 162-172

[3] ANSI/ESD S20.20-2007

[4] Finisar Advanced Optical Components Division," An Atlas of ESD Failure Signatures in Vertical Cavity Surface Emitting Lasers," *Application Note* 2004