

Vixar Application Note

Operation of VCSELs Under Pulsed Conditions

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1 Introduction

This application note will discuss how the optical output power from a Vertical Cavity Surfaced Emitting Laser (VCSEL) can be increased beyond the output power under continuous wave (CW) conditions, when driven under pulsed current conditions. To understand the increase in optical output we must discuss the thermal characteristics of VCSELs. Some guidelines regarding the how the increased peak pulsed power is affected by pulsed width and duty cycle will be provided.

2 Background

A typical Light vs. Current (LI) curve for a VCSEL is illustrated in Figure 1. As the current is increased above the laser threshold current (I_{th}), the output power of a VCSEL will generally increase in a linear fashion and we can measure a slope efficiency (mW/mA) over some operating region, for example from 2 mA to 4 mA of the LI response of Figure 1. However, as the current is increased further the output power reaches a peak or maximum (P_{max}) at a current that is defined as I_{max} . As the current is increased further, beyond I_{max} , the LI curve rolls over. This rollover phenomena is caused by internal junction heating and is known as “Thermal Rollover”. Thus, thermal management is very important for VCSELs and to realize optical output powers beyond P_{max} we must consider the thermal characteristics of VCSELs. VCSELs are generally driven at high levels of current density and thus high levels of thermal flux density within their small volume active-junction regions.

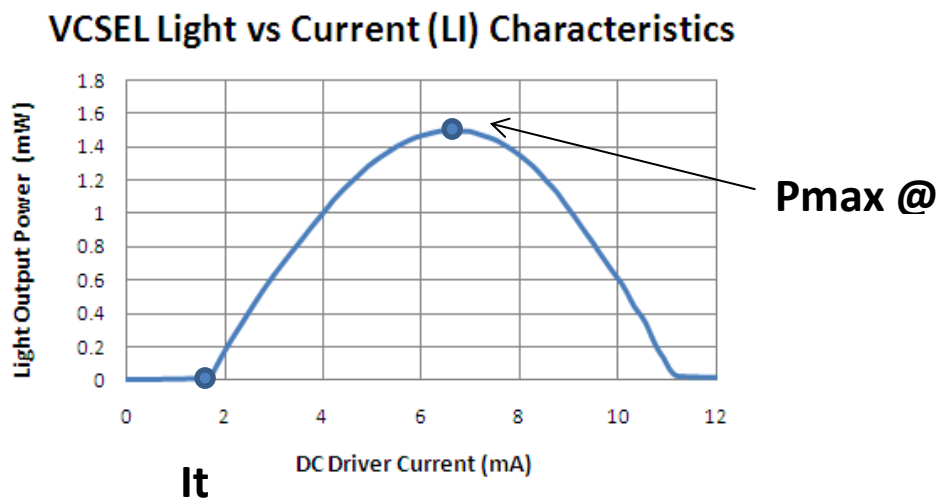


Figure 1: Example of Light vs. Current (LI) Curve for a VCSEL

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3 VCSEL LIV Characteristics over Temperature

Of course, the thermal rollover characteristics of a VCSEL will be dependent on the operating temperature. Examples of the LIV curves for (a) an 850nm multi-mode (MM) VCSEL and (b) a 680nm MM VCSEL are illustrated in Figure 2. It can be seen that as the temperature is increased, P_{max} & I_{max} decrease.

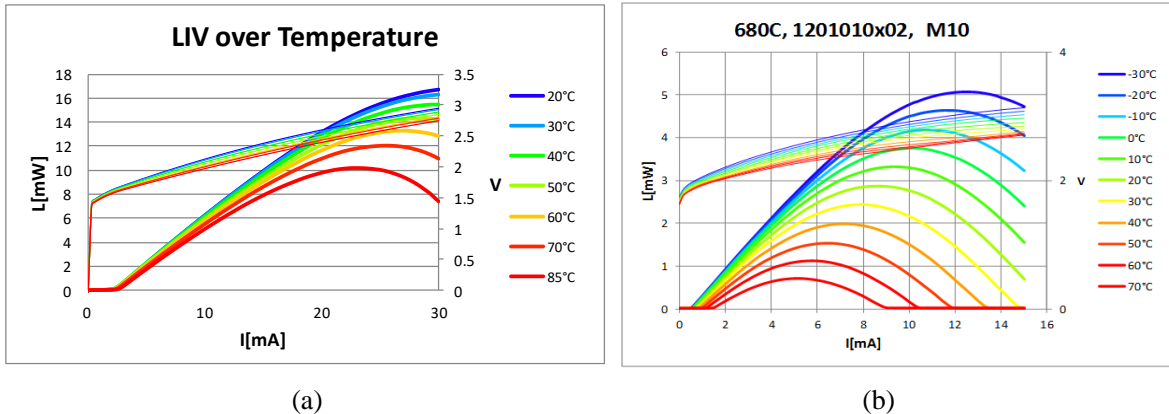


Figure 2: Light Output and Voltage versus Current (LIV) Over Temperature for (a) an 850nm multi-mode VCSEL and (b) a 680 nm multi-mode VCSEL.

4 Increased Optical Power under Pulsed Driver Conditions

The thermal heating of the junction can be reduced by application of short current pulses with a duty cycle less than 100%. The reduced junction heating results in significantly increased optical output power. An example of the peak pulsed power characteristics for a 670 nm single-mode (SM) VCSEL over temperature is provided in Figure 3 for pulsed conditions of 50 ns at 1% duty cycle. Notice that the LI (power L versus current I) curve for the same device under DC or CW operation at 20C is superimposed (Blue Curve). For DC operation P_{max} is about 2 mW at $I_{max} = 7$ mA. When driven under short-pulse low duty-cycle conditions the pulsed thermal roll over point is not reached up to currents of 28 mA, except at the highest temperatures of 100C or 120C.

It should be noted that the peak pulsed power of Figure 3 was measured by using an average power meter, recording the time averaged power, and dividing the average power by the duty cycle to arrive at the peak power.

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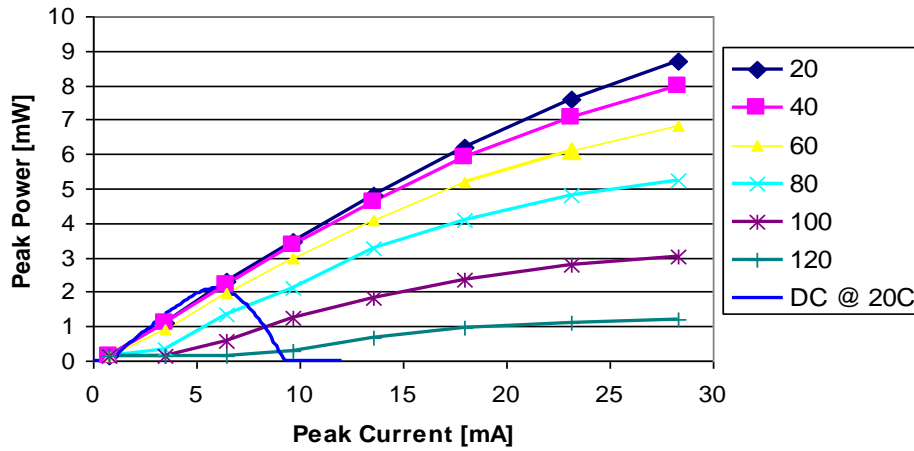


Figure 3: Peak Pulsed Power Characteristics Over Temperature for a 670 nm SM VCSEL

Figure 4 depicts the actual pulsed optical power captured on an oscilloscope using a 350 MHz O/E converter at various pulsed currents. The pulses are 250 ns wide at 1% duty cycle with the different pulses stored in memory and overlaid at various drive current levels. When the optical pulses remain relatively square, calculating the peak power from the average power divided by the duty cycle is quite accurate.

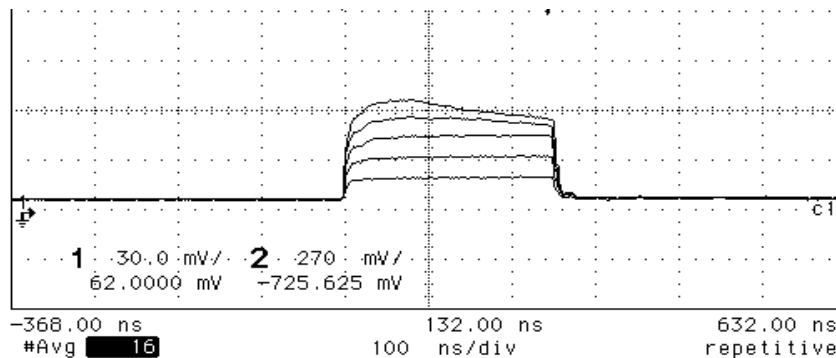


Figure 4: Pulse Shape for multiple current levels at 250nsec pulse width, 1% duty cycle.

5 Effect of Pulse Width & Duty Cycle on Peak Pulsed Power

For short pulse widths (below 250 ns) and low duty cycle (below 5%), it can be shown that the Peak Pulsed Power is essentially independent of either the pulse width or the duty cycle. Figure 5 depicts the actual pulsed optical power captured over a range of pulse widths from 50 ns to 250 ns for a 670 nm Single Mode (SM) VCSEL. Various pulse widths were captured into the scope's memory and overlaid. The data table has the scope memory # (M1 ... M4) and the live

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scope trace, along with the pulse width (T_w) and duty cycle. It can be seen that the peak pulsed power or height of these optical pulses are essentially constant over this operating region.

However, as the pulse width is increased to beyond 1 μ sec, the optical pulses will start to exhibit a droop within each pulse due to intra-pulse heating. Figure 6 illustrates the intra-pulse droop as the pulse widths and duty cycle are both increased. If the peak power were measured using the average power meter, corrected for the duty cycle, then the peak power would be the time averaged peak power across the pulse.

6 Effect of High Pulse Drive Currents

Similar to the droop observed for longer pulse widths and higher duty cycles, droop in the optical pulse can occur for high drive currents. Figure 7 illustrate this effect where the optical pulse droops for pulsed currents of 18.8 and 22 mA.

Optical Pulses Received by a Fiber Coupled O/E

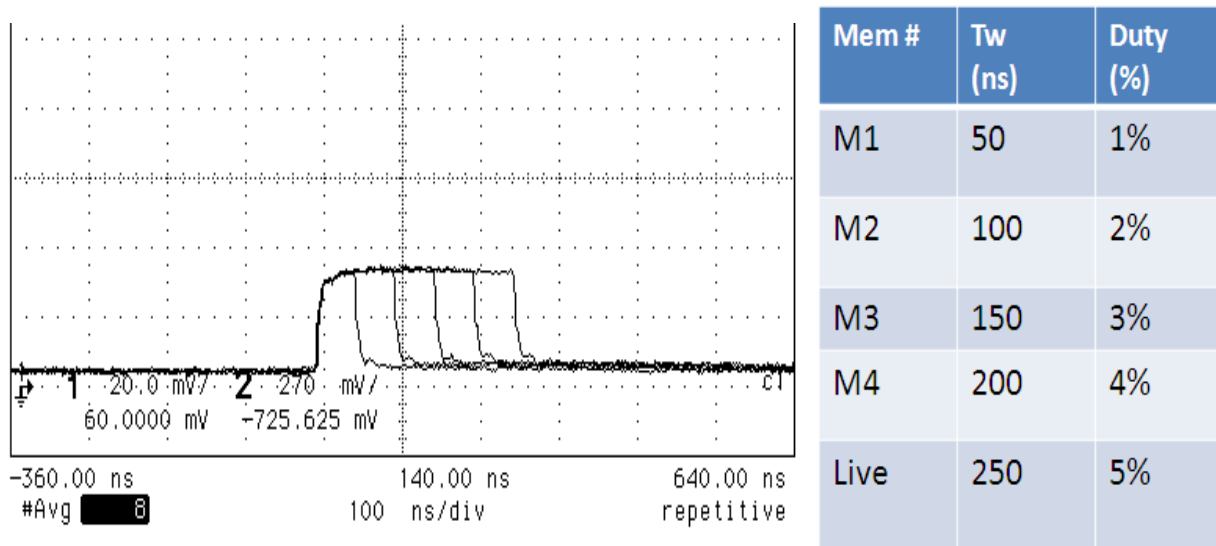


Figure 5: Pulse Shape as a function of pulse width and duty cycle for a fixed current. Pulse widths varied from 50-250nsec and duty cycle varied from 1 to 5%.

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Pulse Width and Duty Cycle Variation @ 5 us Period @

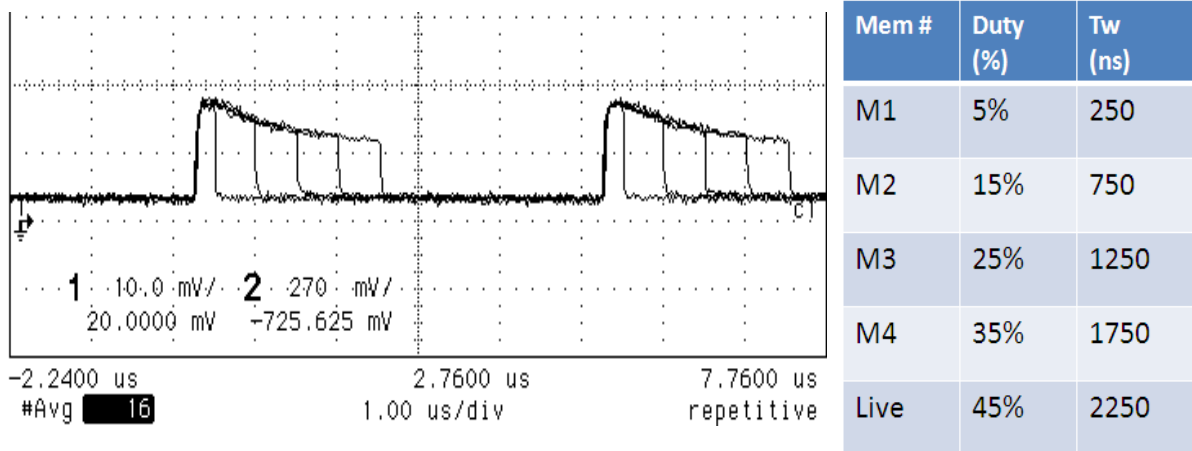


Figure 6: Peak Pulsed Power Droop Characteristics as Pulse Width and Duty Cycle are Increased

Optical Pulse Characteristics vs Driver Current; PW = 250 ns, DC = 5%

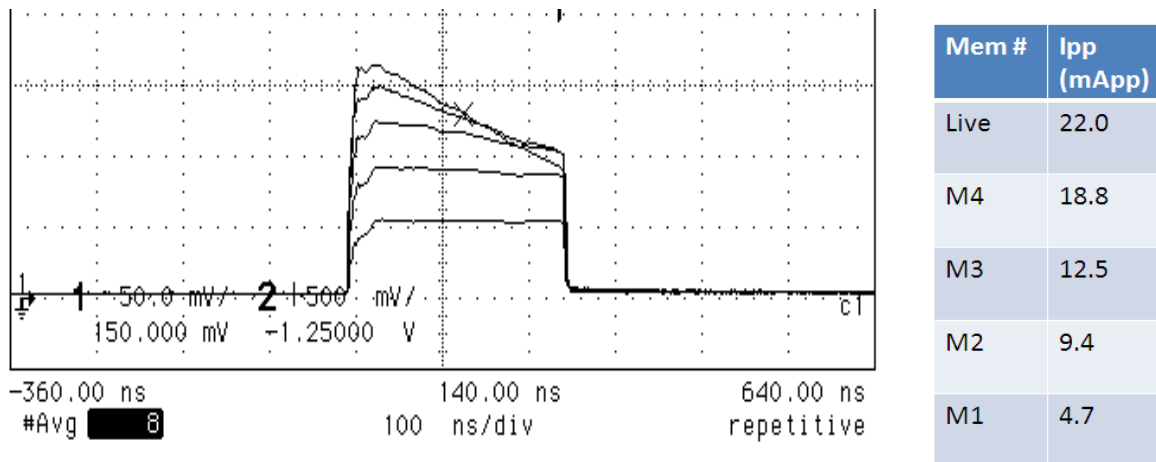


Figure 7: Peak Pulsed Power Characteristics vs. Pulsed Drive Current for a 670 nm SM VCSEL

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7 Variation of Pulse Width and Duty Cycle

We now understand how the pulsed optical signal behaves when driven to high pulsed currents, long pulse widths (1 μ s or higher), and high duty cycles (approaching 50%) and are aware of the optical droop due to intra-pulse heating. Let's examine the pulsed power curves under a fixed duty cycle of 10% when the pulse width is increased from 100 ns to 750 ns as illustrated in Figure 8. Keep in mind that the average optical power meter is performing a time average over the pulse width and that some droop could be present for higher pulse widths and higher currents.

We can also examine the pulsed power characteristics for a fixed pulse width of 500 ns when the duty cycle is varied from 5% to 50% as illustrated in Figure 9.

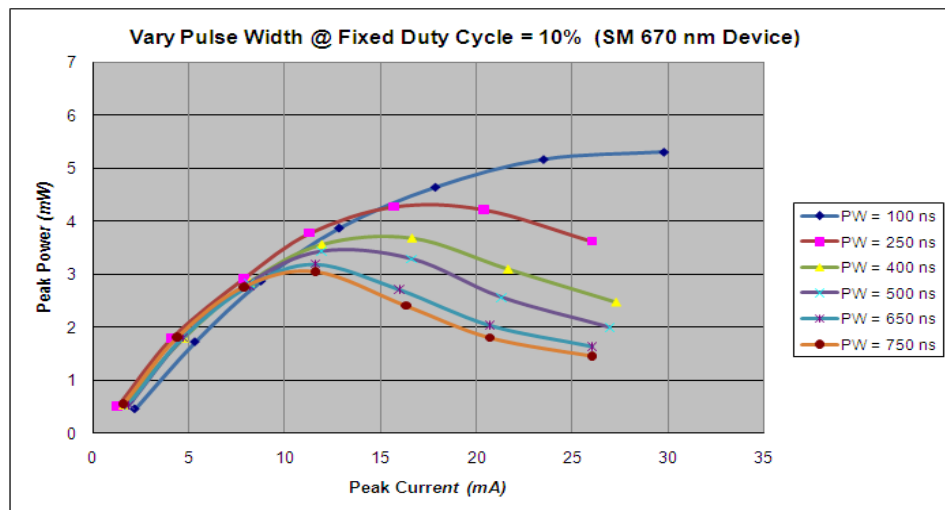


Figure 8: Peak Pulsed Power Characteristics vs. Pulse Width @ 10% Duty Cycle for a 670 nm SM VCSEL

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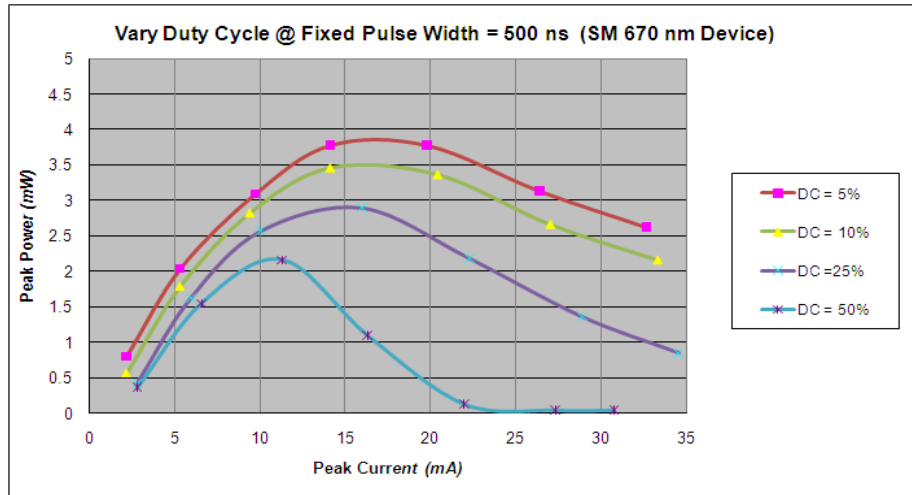


Figure 9: Peak Pulsed Power Characteristics vs. Duty Cycle @ 500nsec Pulse Width for a 670 nm SM VCSEL

8 Dependence on Device Design

Most of the data presented so far, was taken from Vixar's Single Mode (SM) 670nm VCSELs that exhibit peak pulsed power levels between 4 mW and 8 mW, depending on the pulse conditions. However, significantly more pulsed power (20 mW) can be delivered from Vixar's Multi-Mode (MM) VCSELs as illustrated in Figure 10. Again, these pulsed power curves were taken over a range of temperatures (similar to Figure 3).

For comparison, the pulsed characteristics for a smaller Single-Mode device at 500 ns & 10% duty cycle are provided in Figure 11.

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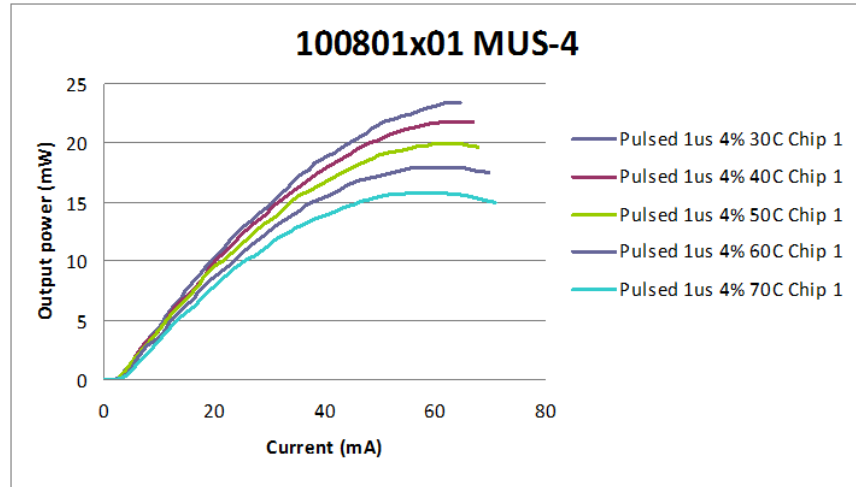


Figure 10: Peak Pulsed Power Characteristics for Vixar's MM VCSELs over Temperature for 1µsec pulse width and 4% duty cycle.

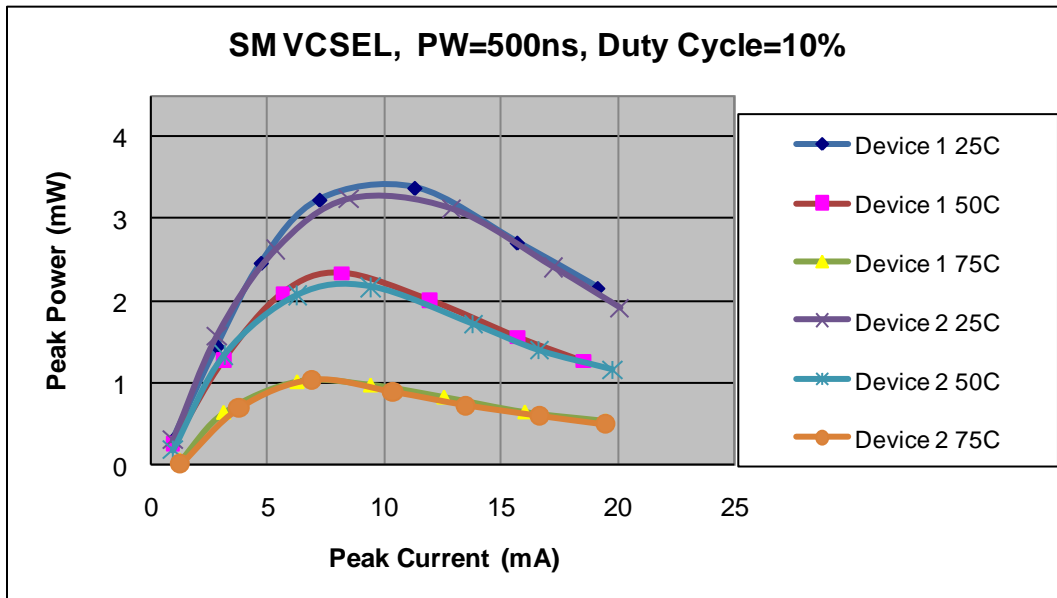


Figure 11: Peak Pulsed Power Characteristics for Vixar's SM VCSEL over Temperature at 500 ns & 10%

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9 Stressed Pulse Testing

All of the previous pulsed power data was taken when driven with purely periodic signals. Some applications, for example laser printers, could require short isolated pulses or bursts of pulses with long periods without any pulses. This is a stressful operating condition due to the potential for a pulse pattern dependency, i.e. the VCSEL output power and turn-on delay can depend upon the pattern of pulses preceding it.

Figure 12 illustrates an example of such stressful pulse streams with four 2 ns pulses in a 10101010 pattern, followed by 246 ns of off time, followed by a single 2 ns pulse. The smaller image on the right is a zoomed in view of the 4 pulses. These pulses were created using a pulsed pattern generator (PPG) and recorded using a high-speed (3 GHz) O/E receiver. A commercial laser driver IC was used to drive the VCSEL. The VCSEL was coupled to a multi-mode optical fiber that routed the optical signal to the O/E receiver. Vixar has measured such pulses with off times up to 1 μ s. To achieve this pattern the driver electronics must be fully DC coupled at the differential input and the VCSEL must be fully DC coupled to the driver output. The VCSEL must be driven hard below threshold to prevent any issues with off state bounce. Notice that the pulsed output levels for the 4 pulses are essentially the same as the level for the single pulse, which is the desired outcome.

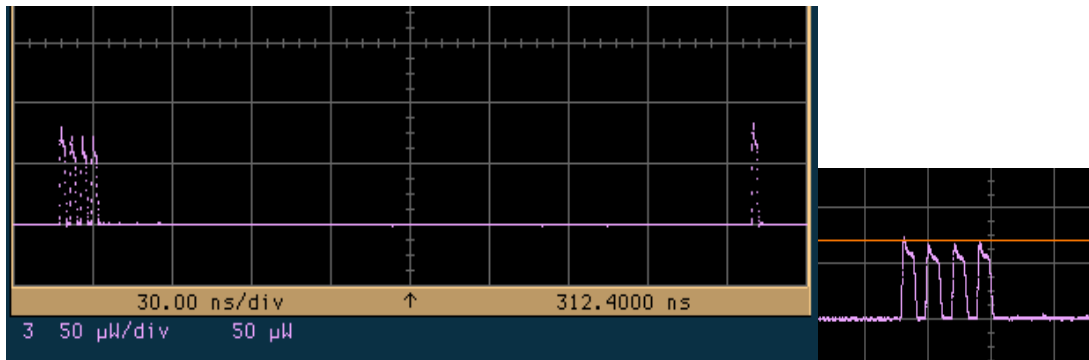


Figure 12: Illustration of Stressed Pulses Testing

10 Modulation at Data Communication Rates (1-10 Gb/s)

An additional question is the shortest pulse width, or speed that the VCSELs can achieve. Using the test set as described in the previous section, 1 Gb/s and 10Gb/s optical signals were recorded using a random test pattern. The optical eye diagrams are provided in Figure 13 for a red VCSEL at 1 and 10Gb/s and an 850nm VCSEL at 10Gb/s. While as expected, some degradation of the eye occurs between 1 and 10Gbps, the openness of the eye is still considered satisfactory for 10Gbps operation.

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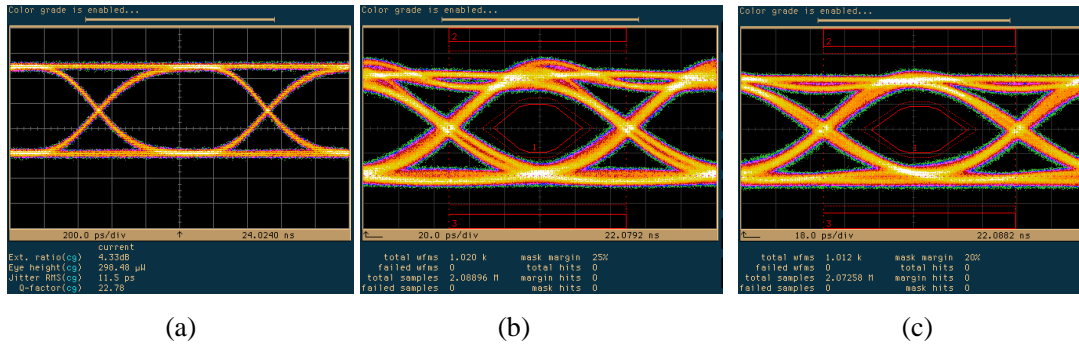


Figure 13: (a) Optical Transmitter Eye Diagram at 1 Gb/s for a 680nm VCSEL, (b) Eye Diagram at 10Gb/s for a 680nm VCSEL, (c) Eye Diagram for an 850nm VCSEL at 10Gb/s/

11 Pulsed Reliability Data

Vixar has accumulated many millions of device-hours of constant current (CW) reliability test data and continually tests existing designs to monitor reliability and new designs to establish the acceleration model. However, the conditions of pulsed operation differ from CW in that higher currents are used, while the pulsed operation might also introduce temperature or stress cycling.

In order to fully understand device reliability when driven under pulsed conditions, Vixar has also undertaken pulsed reliability evaluation. Driver boards were designed and built to pulse each laser with 500 ns pulses at 12.5% duty cycle. Devices were placed under test at 3 temperatures and under 3 different pulsed current levels in a matrix fashion, as typical for reliability testing. Figure 14 provides representative test data for a group of devices operated at 125°C and peak pulsed current of 18mA, for 9000 hours. The devices are periodically removed from the oven and tested CW at a lower current of 8mA, then returned to the ovens. The test conditions correspond to 32 trillion pulse cycles.

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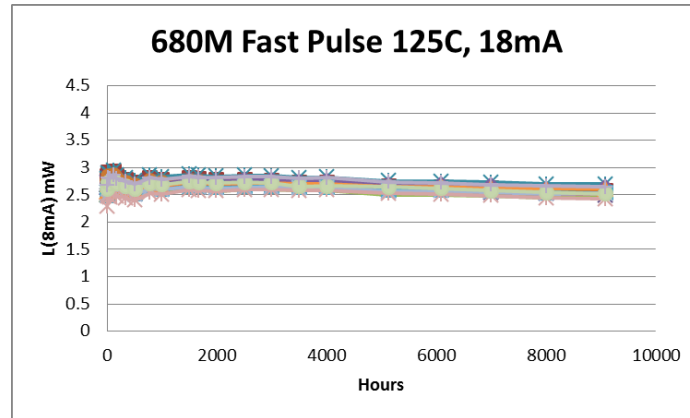


Figure 14: Pulsed Power Reliability Data

12 Conclusions

Extensive VCSEL pulsed-power data has been presented over a range of various pulsed conditions. Since the pulsed power output of a VCSEL is limited by thermal heating of the junction, it is dependent on many factors. These factors include pulse width, pulse duty cycle, temperature, peak pulsed current, and device type. This application note serves as a guide that will help you understand the trends. However, due to the number of variables, it is best to evaluate the VCSEL design of interest under the expected operating conditions to understand the peak power which can be achieved. Vixar can help you optimize device selection, operating temperature range, and operating current range for your pulsed application. Vixar's engineers have many years of experience in VCSEL development, integration with driver circuitry and packaging and can help customers develop complete solutions. Vixar has initiated a pulsed reliability study to ensure that high reliability is maintained for your applications. Please contact Vixar if you would like to discuss this application note or should require some pulsed data at your specific operating conditions.